HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12908A

WRITEABLE CONTROL STORE INTERFACE KIT

(FOR 2100 COMPUTER)

Printed-Circuit Assembly:

12908-60002, Series 1152

Note

This manual should be retained with the applicable computer documentation.

Options Covered

This manual applies to option 001 as well as to the standard version of the HP 12908A Writeable Control Store Interface Kit.

12908-90001

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SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual covers general information, installation, programming, theory of operation, maintenance and replaceable parts for the HP 12908A Writeable Control Store Interface Kit. Option 001 for the interface kit is also covered in this manual.

1-3. GENERAL DESCRIPTION.

1-4. The Hewlett-Packard 12908A Writeable Control Store Interface Kit provides the HP 2100 Computer with the necessary logic to dynamically change the basic instruction set of the computer. Sections II through V of this manual provide installation and programming, theory of operation, maintenance and replaceable parts information for the kit. The printed-circuit assembly and jumper board assembly contained in the interface kits are shown in figure 1-1 and listed in table 1-1. The backplane jumper and manual are not shown in figure 1-1.

1-5. IDENTIFICATION.

1-6. Hewlett-Packard uses five digits and a letter (00000A) for standard kit designations. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office. These offices are listed at the back of this manual.

Table 1-1. Interface Kit Contents

INTERFACE KIT	CONTENTS	HP PART NO.
12908A	Writeable Control Store PCA	12908-60002
	Jumper Board Assembly	12908-60003
	Backplane Jumper Assembly	12908-60005
	Operating and Service Manual	12908-90001
12908A-001	Writeable Control Store PCA	12908-60002

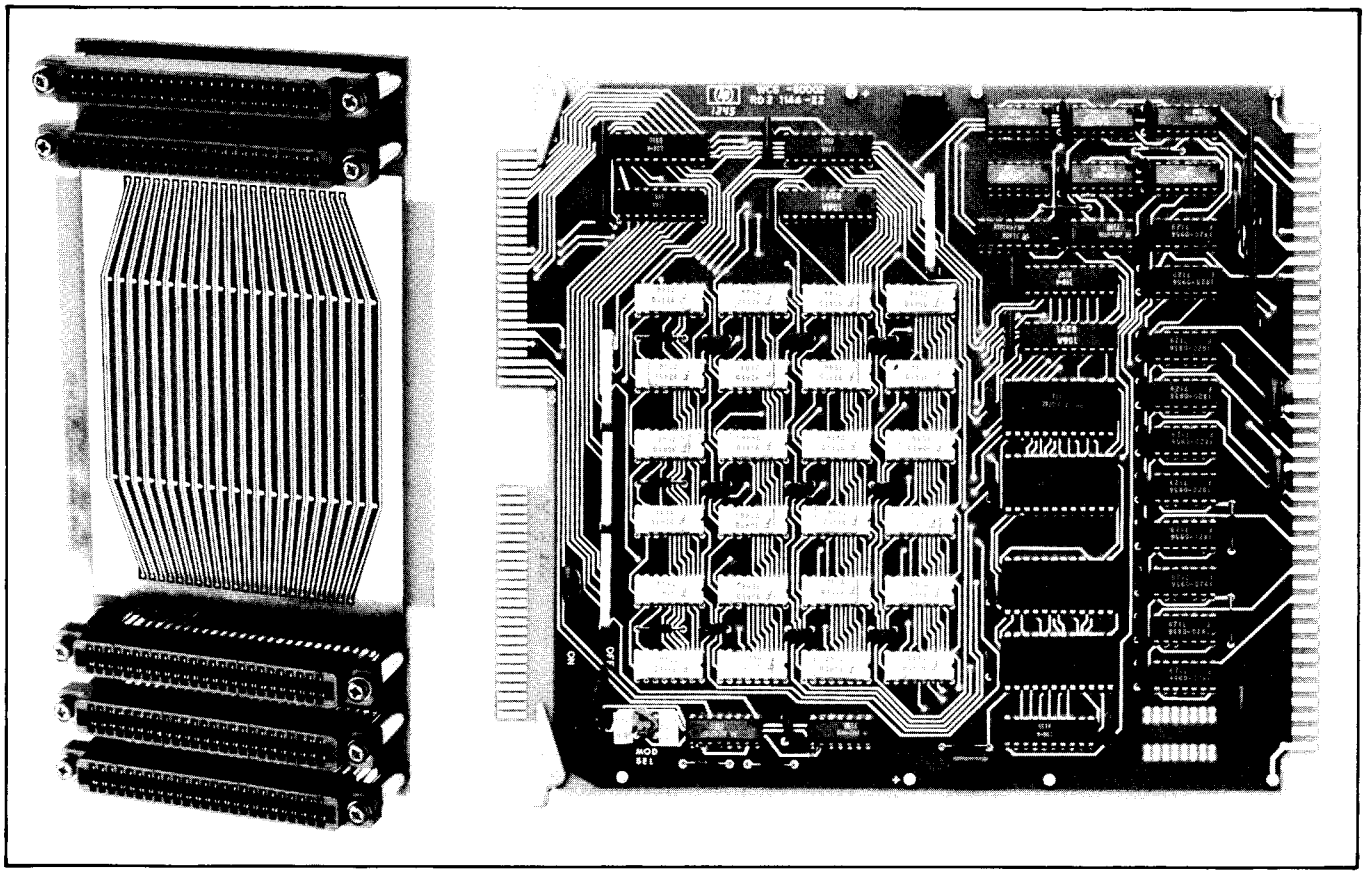


Figure 1-1. Writeable Control Store Interface Kit

1-7. Printed-circuit assembly (PCA) revisions are identified by a letter, a series code, and a division code stamped on the board (e.g., A-1152-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the logic diagram in this manual, there are differences between your PCA and the PCA described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

1-8. Manuals and manual supplements are identified by title and part number on the title page of the doucment.

1-9. OPTIONS.

1-10. Option 001 provides additional writeable control store to the basic kit. This option consists of one writeable control store PCA; specify quantity (up to two per system) when ordering. Also note that it is necessary to have the basic kit before option 001 can be used in the system.

1-11. SPECIFICATIONS.

1-12. Table 1-2 lists the characteristics and specifications of the writeable control store PCA.

Table 1-2. Writeable Control Store PCA Specifications

CAPACITY

Words Available: 256 per module
Maximum WCS Modules: 3 per HP 2100
Word Size: 24-bits
Maximum Primary Entry Points: 16

MICROINSTRUCTION TIME

196 nanoseconds

INSTALLATION

One, two, or three writeable control store PCA's require the use of three Input/Output slots (slots 10, 11, and 12, inclusive). Writeable control store may be used as any module. Module 1, 2 or 3 is normally used. Also available but not recommended by Hewlett-Packard is Module 0, which contains the basic HP 2100 Computer instruction set).

DATA STORAGE

Input/Output Group instructions or via an HP 2100 Direct Memory Access channel (if present).

DATA READBACK

Input/Output Group instructions only.

INTERFACE CURRENT SUPPLIED BY COMPUTER

0.15V (-2V supply); 4.6A (+4.85V supply)

PCA DIMENSIONS

Width: 7-3/4 inches (196.8 mm)
Height: 8-11/16 inches (220.7 mm)

PCA WEIGHT

Net Weight: 18 oz (511.2 gm) (card and cable only)
Shipping Weight: 4 lb (2.27 kg)

PCA INPUT LEVELS

"1" state: 1.9 volts min.
"0" state: 1.1 volts max.

PCA OUTPUT LEVELS

"1" state: 2.4 volts min.
"0" state: 0.7 volt max.

INSTALLATION AND PROGRAMMING

SECTION II

2-1. INTRODUCTION.

2-2. This section provides procedures and information for unpacking and inspection, installation, programming, and reshipment of the writeable control store kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracked, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged item without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. Install the writeable control store kit as follows:

a. Ensure that the computer operates properly prior to installing the writeable control store interface kit.

b. Turn off power at the computer.

c. Remove the top and bottom access covers from the computer. Then remove and discard the front plastic strip from the strengthener on the underside of the top access cover.

d. Remove timing and control PCA A1, part no. 02100-60014, from slot 1 of the computer and verify that the revision data is not A-1116-22. If the revision data is A-1116-22, locate the printed circuit traces connected to pins 38 and 40 of 50-pin connector J1. Cut these traces with a sharp knife so that no electrical contact is made to these pins.*(See CAUTION.)* This action does not affect the operation of the computer in any way. Replace the timing and control PCA in slot 1.

CAUTION

PCA A1 is a multilayer board and can be easily damaged if the traces are carelessly cut.

e. Remove ROM control PCA A2, part no. 02100-60002, from slot 2 of the computer. Refer to table 2-1 and configure jumpers W1 through W6 to the desired number of modules.

Table 2-1. ROM Control PCA A2 Jumper Connections for Various Module Configurations

MODULES INSTALLED (INCLUDING ROM MODULES)	JUMPERS TO BE INSTALLED					
	W1	W2	W3	W4	W5	W6
0	A to B	D to K	E to F	in	out	H to L
0, 1	A to B	none	none	in	out	H to L
0, 2	none	D to K	E to F	out	in	none
0, 3	A to B	C to D	E to F	in	in	G to H
0, 1, 2	A to D	none	E to F	in	out	none
0, 1, 3	A to B	none	none	in	out	G to H
0, 2, 3	none	C to D	E to F	out	in	none
0, 1, 2, 3	none	none	none	in	out	none

f. Replace ROM control PCA A2 in slot 2.

g. Connect backplane jumper assembly, part no. 12908-60005, between pins XA8-70, XA10-72, XA11-72, and XA12-72 on the backplane.

h. On the writeable control store PCA (or PCAs, if installing option -001) place MOD SEL switch S2 in the desired module number position.

i. On the writeable control store PCA, place WCS module 0 enable switch S1 in the OFF position.

j. Place the first writeable control store PCA in slot number 10 (select code 25) of the I/O section of the computer. Any additional writeable control store PCAs should be placed in slots 11 and 12 for select codes 24 and 23, respectively, in that order.

Note: If an I/O extender card, part no. 02155-60003, previously occupied slot 10, it must now be installed in slot 13. Device I/O cards previously occupying slots 11 and 12 must now be installed in the HP 2155A Input/Output Extender. Software must be reconfigured as required to reflect new select code of I/O extender and, if necessary, device I/O cards relocated in HP 2155A. Also, an I/O jumper board, part no. 02116-6110 must be placed in the first slot (select code 25) of the I/O extender.

k. Install the jumper board assembly, part no. 12908-60003, on connector J1 of the writeable control store PCA, connector J1 of ROM control PCA A2, and connector J1 of timing and control PCA A1. (Connector J1 is the connector closest to the front of the computer.)

l. Replace the top and bottom access covers on the computer.

m. Turn on power at the computer and perform the diagnostic test as outlined in the Diagnostic Program Procedures (part no. 12908-90005) contained in the *Manual of Diagnostics*. If the diagnostic program is completed without error, the card is installed and operating properly. If the diagnostic program indicates errors, halt the computer, turn off power and recheck all of the above installation procedures (correct where necessary), then recheck and repeat the operating procedures of the diagnostic.

2-7. RESHIPMENT.

2-8. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-9. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-10. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 Cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N. J. and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note: In any correspondence, identify the kit by model number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-11. PROGRAMMING.

2-12. Two methods exist for writing data into (loading) a writeable control store module: under program control, and via DMA (if available). Under program control, prior to initiating the load routine, the data to be loaded must be stored in the computer memory. This will require a block of up to 512 words per module. The load routine will send two words from memory (32 bits which are mapped into an 8-bit address and a 24-bit microinstruction) to the writeable control store module, issue a write command to that module and cause the data to be stored there. The load routine will repeat this process until the desired number of words have been stored in the writeable control store module.

2-13. Once loaded, the contents of the writeable control store module may be read back under program control via the I/O bus and compared with its counterpart in memory.

2-14. The following is an example of the program sequence necessary for loading writeable control store under program control. This example does not include block pointers, counters, etc., which are necessary for proper control.

Note: "sc" indicates select code of WCS PCA.

STF	sc	Initializes the Direction FF.
OTA	sc	Loads first computer word into first WCS buffer and toggles the Direction FF. This word comprises the eight-bit address and the eight most significant bits of the microinstruction.
OTB	sc	Loads the second computer word into the second WCS buffer and toggles the Direction FF. This word comprises the 16 least significant bits of the microinstruction.
STC	sc	Provides the write pulse to load the WCS buffers into the RAM.

2-15. The OTA, OTB, and STC instructions are normally in a loop that is repeated until the desired number of microinstructions have been stored. OTA/OTB was chosen as an example, any combination of these instructions is allowable.

2-16. An example of reading from writeable control store under program control via the I/O bus is shown below. This example is shown without regard to the block pointers, counters, etc., which are necessary for proper control.

Note: "sc" indicates the select code of the WCS PCA.

STF	sc	Initializes the Direction FF.
OTA	sc	Sends the eight-bit address to the WCS module from the eight most significant bits of the A-register. (B-register could be used.)
STF	sc	Re-initializes the Direction FF.
LIA	sc	Places eight zeros into the eight most significant bit positions of the A-register and places the eight most significant bits of the microinstruction into the eight least significant bit positions of the A-register.
LIB	sc	Places the 16 least significant bits of the microinstruction into the B-register.

2-17. The STF, OTA, STF, LIA, and LIB sequence is normally in a loop that is repeated until the desired number of microinstructions have been read in from writeable control store. LIA/LIB was chosen as an example, any combination of these instructions is allowable.

2-18. Under DMA control, the load routine must send only the three DMA control words to the selected channel. When the channel is turned on, DMA will utilize every memory cycle until the entire block of data is sent to the writeable control store module (maximum of 512 cycles). DMA will transfer these words at a rate of 980 ns/word (512 words will take 502 μs to transfer).

2-19. The following is an example of the program sequence necessary for loading writeable control store via DMA. This example does not include block pointers, counters, etc, which are necessary for proper control.

Note: "sc" indicates the select code of the WCS PCA.

```
LDA   CW1   Get the first DMA control word.
OTA   6     Send the first DMA control word to
            the selected DMA channel. (DMA
            channel 1 has been selected here for
            demonstration purposes only.)
CLC   2     Prepare the selected DMA channel to
            receive the second DMA control word.
LDA   CW2   Get the second DMA control word.
STC   2     Prepare the selected DMA channel to
            receive the third DMA control word.
OTA   2     Send the second DMA control word to
            the selected DMA channel.
LDA   CW3   Get the third DMA control word.
OTA   2     Send the third DMA control word to
            the selected DMA channel.
STC   6,C   Turn on the selected DMA channel.
STF   sc    Initialize the Direction FF.
CLF   sc    Start the DMA transfer.
SFS   6     Test for the completion of the
            transfer.
JMP   *-1   Loop until done.
CW1   OCT   12000sc
CW2   OCT   Starting address of the block to be
            transferred.
CW3   OCT   Two's complement of the number of
            computer words to be transferred.
```

SECTION III THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section presents the theory of operation of writeable control store within the HP 2100 Computer. A logic diagram, parts location diagram and replaceable parts list are located in section IV of this manual.

3-3. WRITEABLE CONTROL STORE OPERATION.

3-4. Writeable Control Store (WCS) consists of a bipolar semiconductor Random Access Memory (RAM) containing 24 integrated circuit (IC) packages along with the necessary cables and electronics mounted on a 2100-size printed-circuit assembly which can be inserted into any of the computer I/O slots. However, if the jumper board assembly (part no. 12908-60003) supplied by HP is used, only slot 10, 11 and 12 can be used, Each IC package is configured in 256 bits organized as one bit per word. Thus one module of WCS is capable of storing 256 words of 24 bits each. Up to three modules of WCS may be installed in a HP 2100A Computer.

3-5. For proper addressing of WCS, a selector switch on the WCS PCA must be set to identify that PCA as a particular module of control store (module 0, 1, 2, or 3). For example, if the switch is set to M2 (module 2), the PCA will be enabled when the ROM Address Register (RAR) contains the pattern "10" in its two most significant bits (bits 9 and 8), and disabled otherwise. When enabled, the word in WCS addressed by RAR bits 0 through 7 will be sent to the ROM Instruction Register (RIR) as signals ROM0 through ROM23. The computer will then execute this word (microinstruction) as though it came from the basic computer instruction set in the control store on ROM control PCA A2 (module 0). The access time of data from WCS (140 ns) allows the computer to operate at its normal clock rate (196 ns). If it is desired to operate WCS as module 0, the WCS module 0 switch (S1) on the WCS PCA must be set to the ON position and the selector switch to M0 (see note following). This enables WCS as module 0 and inhibits the control store module 0 on ROM control PCA A2. If the computer contains a module in ROM other than module 0 (for example, if floating point is installed as module 1 on the ROM control PCA) and it is desired to operate WCS as that module, the ROM integrated circuits must be removed from the ROM control PCA in order to prevent unwanted "or" conditions of the data lines (ROM0 through ROM23).

Note: Switch S1 must be set to the OFF position while WCS is being loaded. The computer must be halted following the load, at which time switch S1 is set to the ON position. The computer may then be operated using the WCS module 0 as its basic control store.

3-6. WCS also consists of the software which allows it to be used as a dynamically microprogrammed control store for the HP 2100 Computer. This software includes an assembler for converting the microcode to machine code, a driver to load the machine code into WCS and verify the load, and a mask generator to produce the tapes necessary to produce ROMs, if desired. An operating system is also provided for altering the contents of WCS during the debug phase.

3-7. The WCS PCA plugs into any of the I/O slots of the HP 2100 Computer (slots 10, 11, and 12 are recommended; see paragraph 2-6) and can be used as a replacement for, or an extension of the existing ROM control store. Up to three PCAs may be used per computer to give a maximum of 768 by 24 bits of WCS words.

3-8. Writeable control store is connected to the computer central processor through the I/O structure (for loading and checking), and also through a 50-wire PCA connector. It is this connector that enables writeable control store to be used as an extension of the computer's basic control store. The cable connects one or more (maximum of three) writeable control store PCAs to ROM control PCA A2 and timing and control PCA A1. The ROM address register on PCA A2 sends a 10-bit address to the writeable control store PCA or PCAs through this cable, and the addressed PCA then sends its data (microinstruction) from that address back through the cable. The cable is terminated on PCA A2 where the 24 data lines (ROM0 through ROM23 are "or" tied onto the corresponding outputs of the basic control store. From there the data is sent to the ROM instruction register as though it was from the basic control store.

3-9. For the purpose of execution of WCS instructions, WCS can be configured to be addressed as any one of the computer's four ROM modules including module 0. However, when configured as module 0, the basic ROM module 0 is disabled.

3-10. To load the WCS RAM circuits, the WCS PCA must be addressed through the I/O interfacing structure of the computer. A 32-bit format is necessary, requiring that a 2-word transfer through the machine A and/or B registers be used in the loading procedure. Two computer words and thus two transfer operations are required for one WCS word. The eight most significant bits of the first computer word transferred is the WCS RAM circuit address where the remaining eight bits of the first computer word and all 16 bits of the second computer word (total 24 bits) will be stored.

3-11. Once loaded, WCS becomes an extension of the ROM via the ROM control PCA. Thus the WCS may be

used to alter the computer instruction set while the computer is in an operating condition. This feature permits dynamic expansion of the computer instruction set.

3-12. DETAILED THEORY.

3-13. COMPUTER POWER ON.

3-14. When power is initially applied by the POWER switch on the computer, the POPIO signal is applied at time T5 to the WCS PCA at pin 17. This signal causes the SRQ FF to clear and the DIR FF to set.

3-15. LOADING OPERATION.

3-16. To explain the loading operation of WCS, use will be made of the loading program described in section II of this manual, the WCS loading timing diagram (figure 3-1), and the logic diagram (figure 4-2).

3-17. The first instruction of the program is the STF instruction. This instruction causes the signal STF to be generated at time T3 and applied to pin 9 of the WCS PCA. This signal, along with the proper select code, causes the SRQ FF to clear and the DIR FF to set. The first output instruction is then issued, generating the signal IOO. Signal IOO is applied to pin 20 of the WCS PCA and it, along with the proper select code, causes the data on the IOB lines (first computer word to be transferred) to be gated into the RAM address register and the eight most significant bits of the RAM data register. The IOO signal also causes the TGL FF to be set at time T3, which causes the DIR FF to be cleared as soon as signal IOO goes low at time T5. The second output instruction again causes signal IOO to be generated, gating the second computer word into the 16 least significant bits of the RAM data register. This second IOO signal again sets the TGL FF at time T3 causing the DIR FF to be set. The STC instruction causes the signal STC to be generated, setting the CTL FF and gating the 24 bits of data in the WCS data register into the addressed WCS RAM location at time T5. This one location in the WCS RAM is loaded with 24 bits from the computer.

3-18. CHECKING OPERATION.

3-19. The checking operation of WCS is essentially the same as the loading operation except that the signal IOI is generated by the two output instructions, causing the DIR FF to be toggled and RAM bits 0 through 24 to be gated at the appropriate times onto the IOB lines.

3-20. DMA OPERATION.

3-21. The direct memory access (DMA) function of the computer provides a direct data path between the computer memory and writeable control store (WCS) via software selection. During a DMA data transfer, the central processor is disabled and the DMA circuits supply the required control signals to operate the memory and WCS. Consecutive memory cycles can be utilized by DMA, allowing a maximum data transfer rate of one million words per second. DMA data transfers are accomplished in blocks, with the block length specified by software. Maximum block length for WCS is 512 computer words. The DMA circuits can be programmed to interrupt at the end of a data block transfer to a subroutine to re-initialize DMA for another data block transfer facilitating the successive loading of successive WCS modules.

3-22. DMA INITIALIZATION. Three control words are used to initialize a DMA channel. The control words are briefly described as follows:

a. Control Word 1 (CW1). Specifies the select code of the I/O device to provide or receive data (bits 0 through 5) and if CLC (bit 13) or STC (bit 15) signals are to be provided to the I/O interface after each word transfer.

b. Control Word 2 (CW2). Specifies input or output DMA operation (bit 15) and the starting address in memory (bits 0 through 14) of the data block.

c. Control Word 3 (CW3). Specifies the length of the data block (bits 0 through 15) and is expressed in two's-complement form.

3-23. All three control words are transferred to the DMA circuits via the S-bus.

3-24. Control Word 1 is loaded into the DMA service select register, CLC Select FF, and STC Select FF by an OTA 06 instruction. Control words 2 and 3 are both loaded into their respective registers by an OTA 02 instruction. A programmed CLC 02 clears the register load control and enables the S-bus data to the memory address register and the In/Out Select FF. An OTA 02 instruction with Control Word 2 in the computer A-register then transfers the control word to its respective registers. Prior to transferring Control Word 3, an STC 02 instruction sets the register load control and enables the S-bus data to the word count register. Another OTA 02 instruction with Control Word 3 in the computer A-register transfers the two's complement of the data block length to the word count register.

3-25. The last step to initialize the DMA circuits is accomplished by an STC 06 instruction. This sets the DMA Control FF and the Transfer Enable FF. The Control FF in the set state enables the DMA interrupt logic and must be cleared by a CLC 06 instruction if an interrupt at the end of a data block transfer is not desired. The Transfer Enable FF in the set state enables the set input to the Cycle Request FF.

3-26. The channel-one DMA circuits are now initialized and a service request from WCS will initiate the first DMA cycle. Channel-two initialization is identical except for the select codes used to address the channel. For initialization of channel-two, select code 03 replaces select code 02 and select code 07 replaces select code 06.

3-27. The DMA cycle is initiated when WCS, with a true SRQ signal, that it is ready for data transfer. The SRQ

selector provides a true Service Request to the Cycle Request FF. The Cycle Request FF is clocked to the set-state by the leading edge of SIR signal at T5 and the PH5 FF is clocked to the set-state by the trailing edge of the SIR signal (at the beginning of T6). The SPH5 signal to the control section causes the central processor to freeze at I/O time T6 to prevent further processing of programmed instructions until the DMA cycle is complete. The DMA cycle begins at T6 and continues until the PH5 FF is cleared at the next time T6. At T6 during the DMA cycle, the memory address register output is strobed onto the S-bus and at the end of this time T6, the memory address register and the word count register are incremented for the next DMA cycle.

3-28. Control signals generated by the DMA circuits perform the following operations during a DMA output operation:

a. Signal RW, at time T6, initiates a memory section read-write cycle to begin at time T2.

b. Combined true STORE and SELM signals, at time T6, load the S-bus data into the memory section M-register.

c. Combined true READ and SELT signals, at time T4T5, transfer memory section T-register data to the S-bus.

d. Signal SIOB, at time T4T5, transfers the S-bus data, via the I/O-bus, to the WCS address and data registers.

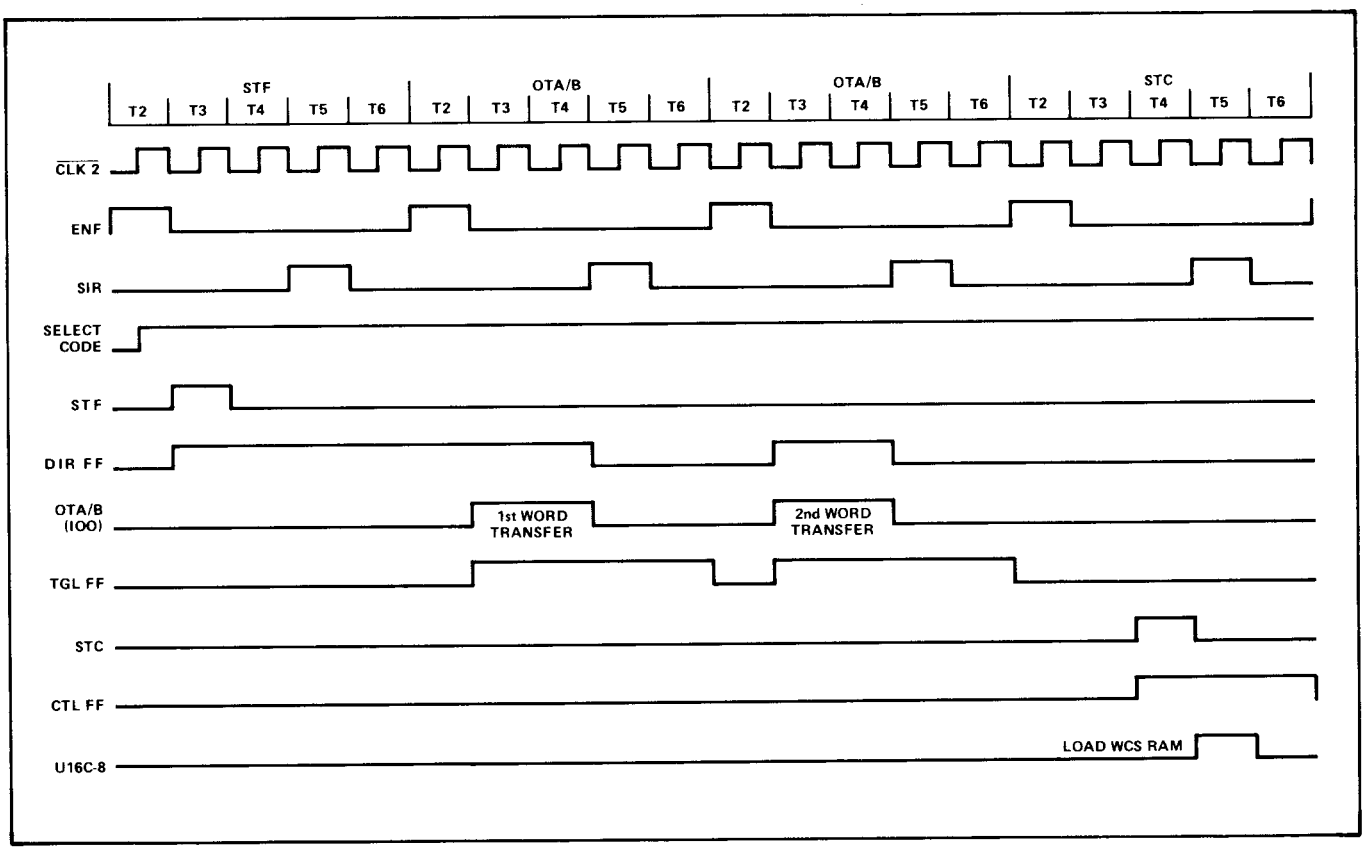
e. Signal CLF, at time T3 ensures that the WCS SRQ signal will remain true to guarantee that WCS will steal the next cycle. This allows the 1-MHz transfer rate.

f. Signal STC, at time T3, if selected, signals WCS to accept data.

3-29. END DATA TRANSFER. As stated, the word count register is loaded with the two's complement of the data block length. The word count register is incremented every DMA cycle so that during the last cycle of the data block, a carry is generated out of the last stage (bit 15) of the word count register. This carry, designated Word Count Rollover (WCR), clears the Transfer Enable FF and sets the Flag Buffer FF. The Transfer Enable FF, in the clear state, inhibits any further service requests to the Cycle Request FF. The Flag Buffer FF, in the set state, initiates the DMA interrupt logic.

3-30. At time T2 during the last DMA cycle, the Flag FF sets; if the Control FF is set, the IRQ FF sets at time T5. Signals FLG and IRQ from the IRQ FF initiate an I/O interrupt to the DMA channel interrupt address (00006 or 00007). A DMA interrupt service routine may then be used to re-initialize the DMA channel for another data block transfer.

3-31. With a CLC in control word one, the roll-over will also force DMA to issue a CLC to WCS, thereby clearing the SRQ FF.



2199-5

Figure 3-1. WCS Loading Timing Diagram

4-1. INTRODUCTION.

4-2. This section contains information on diagnostics and troubleshooting for the writeable control store kit.

4-3. PREVENTIVE MAINTENANCE.

4-4. Preventive maintenance for the writeable control store kit should be performed when the preventive maintenance routines for the computer system are performed. Preventive maintenance consists of inspecting the writeable control store PCA and jumper board assembly for burned or broken components, loose connections, and deteriorated insulating materials.

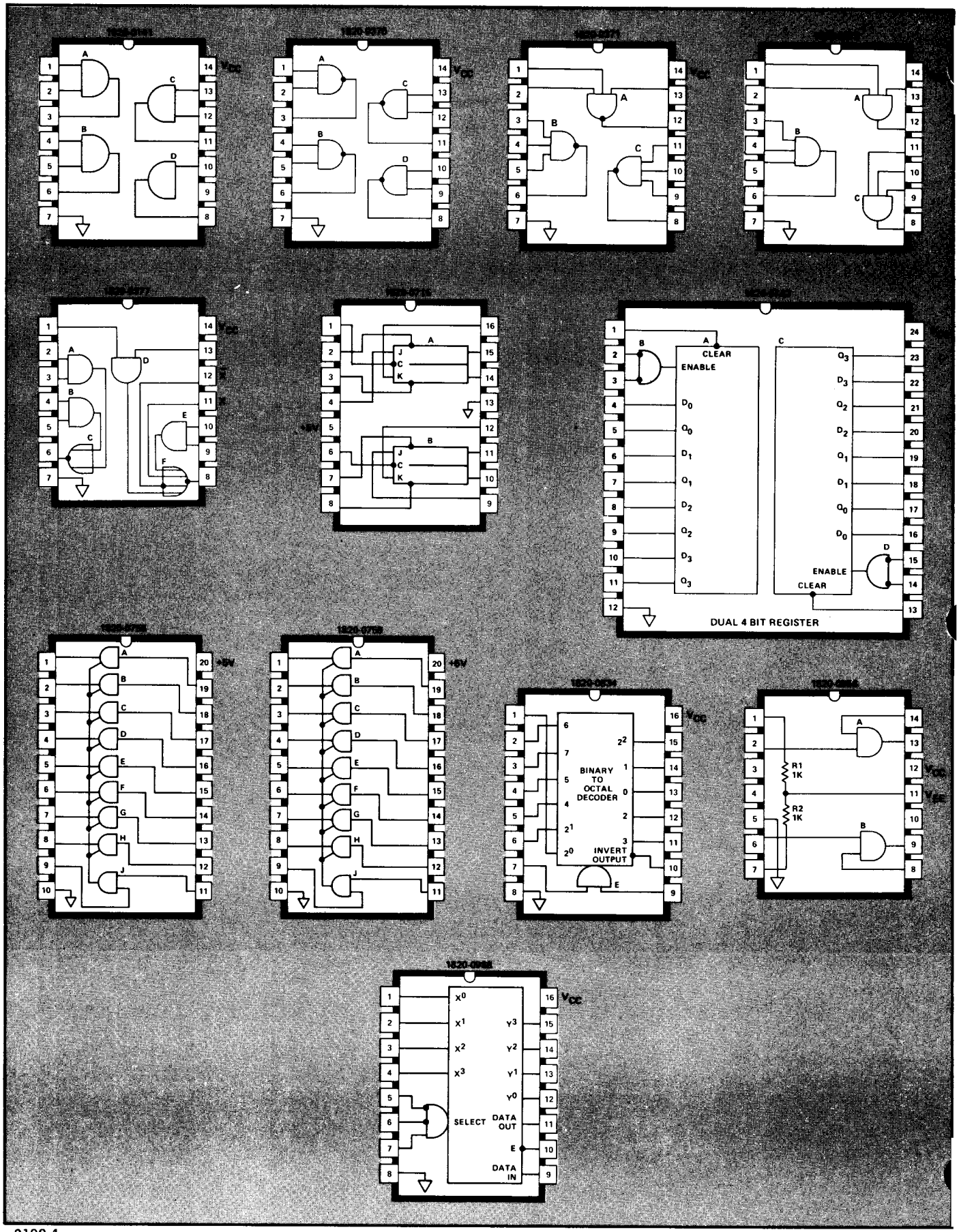
4-5. TROUBLESHOOTING.

4-6. Troubleshooting for the writeable control store interface kit is accomplished by performing the tests in the diagnostic program and analyzing any error messages that occur as the test is being run. Paragraph 1-4 lists the items that make up the writeable control store interface kit. Table 4-1 contains a replaceable parts list for the writeable control store PCA with parts listed in alphanumeric order by reference designation. Figure 4-1 illustrates the internal layout of the integrated circuits used in this kit. Figure 4-2 contains a logic diagram and parts location diagram of the writeable control store PCA.

Note: If it is necessary to extend the WCS PCA from the computer for troubleshooting purposes, two extender PCA's, part no. 02116-63216, are necessary. One extender is used to extend the WCS PCA and one extender is used to extend ROM control PCA A2.

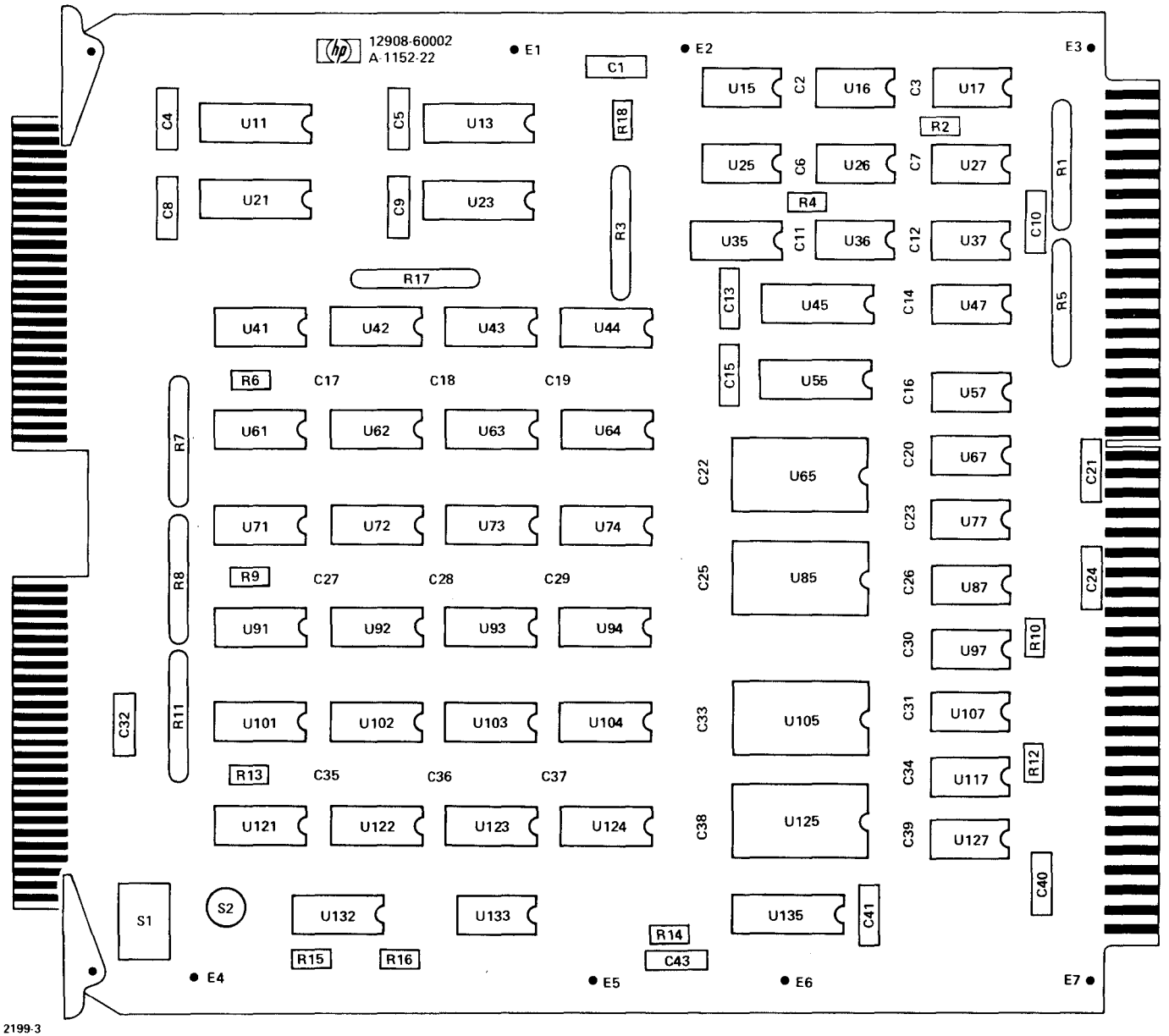
Table 4-1. Writeable Control Store PCA, Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 10, 21, 24, 32, 40, 43	0160-3901	CAPACITOR, Cer, 2.2 uf, ±20%, 25 Vdcw	13606	5C120-CML
C2, 3, 6, 7, 11, 12, 14, 16-20, 22, 23, 25-31, 33-39, 42	0160-2055	CAPACITOR, Cer, 0.01 uf, -20% +80%, 100 Vdcw	13606	C023F101F103ZS 22-CDR
C4, 5, 8, 9, 13, 15, 41	0150-0121	CAPACITOR, Cer, 0.1 uf, -20% +80%, 50 Vdcw	13606	5C50B1-CML
E1-7	0360-0294	TERMINAL	88245	2010B-2
R1, 5, 17	1810-0030	RESISTOR, NETWORK, 1K, 5%, 0.15W	13606	200C1618-CRR
R2	0698-0082	RESISTOR, fxd, film, 464 ohms, 1%, 1/8W	19701	MF4CT-0
R3, 7, 8, 11	1810-0080	RESISTOR NETWORK, 500 ohms, 5%, 0.15W	13606	200 Series
R4, 14, 16, 18	0757-0280	RESISTOR, fxd, film, 1K, 1%, 1/8W	19701	MF4CT-0
R6, 9, 13	0757-0427	RESISTOR, fxd, film, 1.5K, 1%, 1/8W	19701	MF4CT-0
R10, 12	0698-3441	RESISTOR, fxd, film, 215 ohms, 1%, 1/8W	19701	MF4CT-0
R15	0698-3444	RESISTOR, fxd, film, 316 ohms, 1%, 1/8W	19701	MF4CT-0
S1	3101-1213	SWITCH, DPST-DB, 0.5a, 28 Vdc	81640	T8001
S2	3100-2687	SWITCH, SPST, 6 position, 100 ma, 28 Vdc	73138	374H
U11, 13, 21	1820-0755	INTEGRATED CIRCUIT, TTL	28480	1820-0755
U15	1820-0377	INTEGRATED CIRCUIT, TTL	01295	SN4485
U16	1820-0371	INTEGRATED CIRCUIT, TTL	01295	SN4479
U17, 26, 36, 133	1820-0370	INTEGRATED CIRCUIT, TTL	01295	SN4478
U23, 45, 55, 135	1820-0759	INTEGRATED CIRCUIT, TTL	28480	1820-0759
U25	1820-0372	INTEGRATED CIRCUIT, TTL	01295	SN4480
U27	1820-0141	INTEGRATED CIRCUIT, TTL	04713	SC7514PK
U35	1820-0715	INTEGRATED CIRCUIT, TTL	01295	SN33510
U37, 47, 57,	1820-0956	INTEGRATED CIRCUIT, CTL	17803	SL3459
67, 77, 87, 97, 107, 117, 127	1820-0988	INTEGRATED CIRCUIT, TTL	17803	SL40850
U41-44, 61-64, 71-74, 91-94, 101-104, 121-124	1820-0988	INTEGRATED CIRCUIT, TTL	17803	SL40850
U65, 85, 105, 125	1820-0742	INTEGRATED CIRCUIT, TTL	17803	SL17869
U132	1820-0834	INTEGRATED CIRCUIT, TTL	04713	SC18951PK



2199-4

Figure 4-1. Integrated Circuit Diagrams


12908-60002
A-1152-22
E1
E2
E3
E4
E5
E6
E7
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40
C41
C43
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
S1
S2
U11
U13
U15
U16
U17
U21
U23
U25
U26
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U35
U36
U37
U41
U42
U43
U44
U45
U47
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U57
U61
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U63
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U67
U71
U72
U73
U74
U77
U85
U87
U91
U92
U93
U94
U97
U101
U102
U103
U104
U105
U107
U117
U121
U122
U123
U124
U125
U127
U132
U133
U135
2199-3

WRITEABLE CONTROL STORE (12908-60002, SERIES 1152)

ADDRESS BUFFER U23

RAR0 J1.33 — R18 1K +4.85V
RAR1 J1.31 — R17F 1K +4.85V
RAR2 J1.29 — R17E 1K +4.85V
RAR3 J1.23 — R17A 1K +4.85V
RAR4 J1.22 — R17B 1K +4.85V
RAR5 J1.21 — R17D 1K +4.85V
RAR6 J1.19 — R17C 1K +4.85V
RAR7 J1.17 — R17G 1K +4.85V

-2V 47,48 — C10,C24, C40 2.2 (3) — -2V
GND 1,2 / 85,86 — C1,C21 C32,C43 2.2 (4); C2,C3,C6,C7, C11,C12,C14, C16,C20,C22, C23,C25,C31, C33,C39 0.01 (29); C4,C5,C8, C9,C13, C15,C41 0.1 (7)
+4.85V 39,40 — +4.85V

SCM 14 — U25B
SCL 16
IOG 15
STC 22 — R1B 1K, R1C 1K, R1D 1K (-2V)
ENF 46
SIR 32 — R5E 1K, R5A 1K (-2V)
IOO 20 — R1A 1K (-2V)
IOI 24 — R5C 1K (-2V)
STF 9 — R1F 1K (-2V)
POPIO 17 — R1E 1K (-2V)
CLC 21 — R5F 1K (-2V)
CLF 7 — R1G 1K (-2V)

U26C, U26D, U27A, U27D, U27C, U15 (E, F, NC, D), U27B, U17C, U17D, U17A, U16B, U17B

CONTROL FF — U36A, U36B
TOGGLE FF — U26A, U26B
SRQ FF — U16B, U17B

U16C → RAM WRITE ENABLE (TO SHEET 2)
U36C, U36D
R14 1K +4.85V
R4 1K +4.85V
DIR FF U35A
U37A — R5D 1K -2V
U16A

ADDRESS BUFFER U135

RAM ADDRESS REGISTER — U125
RAM MICRO-INSTRUCTION REGISTER — U85, U105

RAM CIRCUITS DATA IN (TO SHEET 2)
BIT 19, BIT 18, BIT 22, BIT 23, BIT 8, BIT 9, BIT 14, BIT 13, BIT 21, BIT 16, BIT 17, BIT 20, BIT 12, BIT 10, BIT 15, BIT 11

IOB4, IOB7, IOB6, IOB1, IOB0, IOB2, IOB3, IOB5, IOB11, IOB13, IOB14, IOB15, IOB10, IOB9, IOB8, IOB12

SRQ 19
IOB 12 8 9 10 — 57 54 56 58
IOB 15 14 13 11 — 74 65 61 60
IOB 5 3 2 0 — 51 45 41 35
IOB 1 6 7 4 — 38 53 52 42

NOTES:
1. RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN UF UNLESS OTHERWISE SPECIFIED.

SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R1, R5, AND R17
A 1K, B 1K, C 1K, D 1K, E 1K, F 1K, G 1K

SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R3, R7, R8, AND R11
A 500, B 500, C 500, D 500, E 500, F 500, G 500

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X0
X1
X2
X3
Y0
Y1
Y2
Y3
RAM X- AND Y-AXIS (TO SHEET 2)
TO U25C-9 (SHEET 3)

ADDRESS BUFFER
U135
U16A

RAM CIRCUITS DATA IN (TO SHEET 2)
BIT 19 BIT 18 BIT 22 BIT 23 BIT 8 BIT 9 BIT 14 BIT 13 BIT 3 BIT 2 BIT 6 BIT 7
BIT 21 BIT 16 BIT 17 BIT 20 BIT 12 BIT 10 BIT 15 BIT 11 BIT 5 BIT 0 BIT 1 BIT 4

RAM ADDRESS REGISTER
RAM MICRO-INSTRUCTION REGISTER
U125 U85 U105 U65

+4.85V
R14 1K
R5B 1K
-2V
R4 1K
R5D 1K

CONTROL FF
U36A U36B
TOGGLE FF
U26A U26B
SRQ FF
U16B U17B
DIR FF
U35A

RAM WRITE ENABLE (TO SHEET 2)

IOB4 IOB7 IOB6 IOB1 IOB0 IOB2 IOB3 IOB5 IOB11 IOB13 IOB14 IOB15 IOB10 IOB9 IOB8 IOB12
RAM OUTPUT BUFFER (FROM SHEET 3)

DIRFF (TO U37B-6)
DIRFF (TO U47B-6)
(TO SHEET 3)
IOI(B) (TO U47A-14)

SRQ
IOB 12 8 9 10
IOB 15 14 13 11
IOB 5 3 2 0
IOB 1 6 7 4

Figure 4-2. Writeable Control Store PCA, Parts Location and Schematic Diagrams (Sheet 1 of 3)

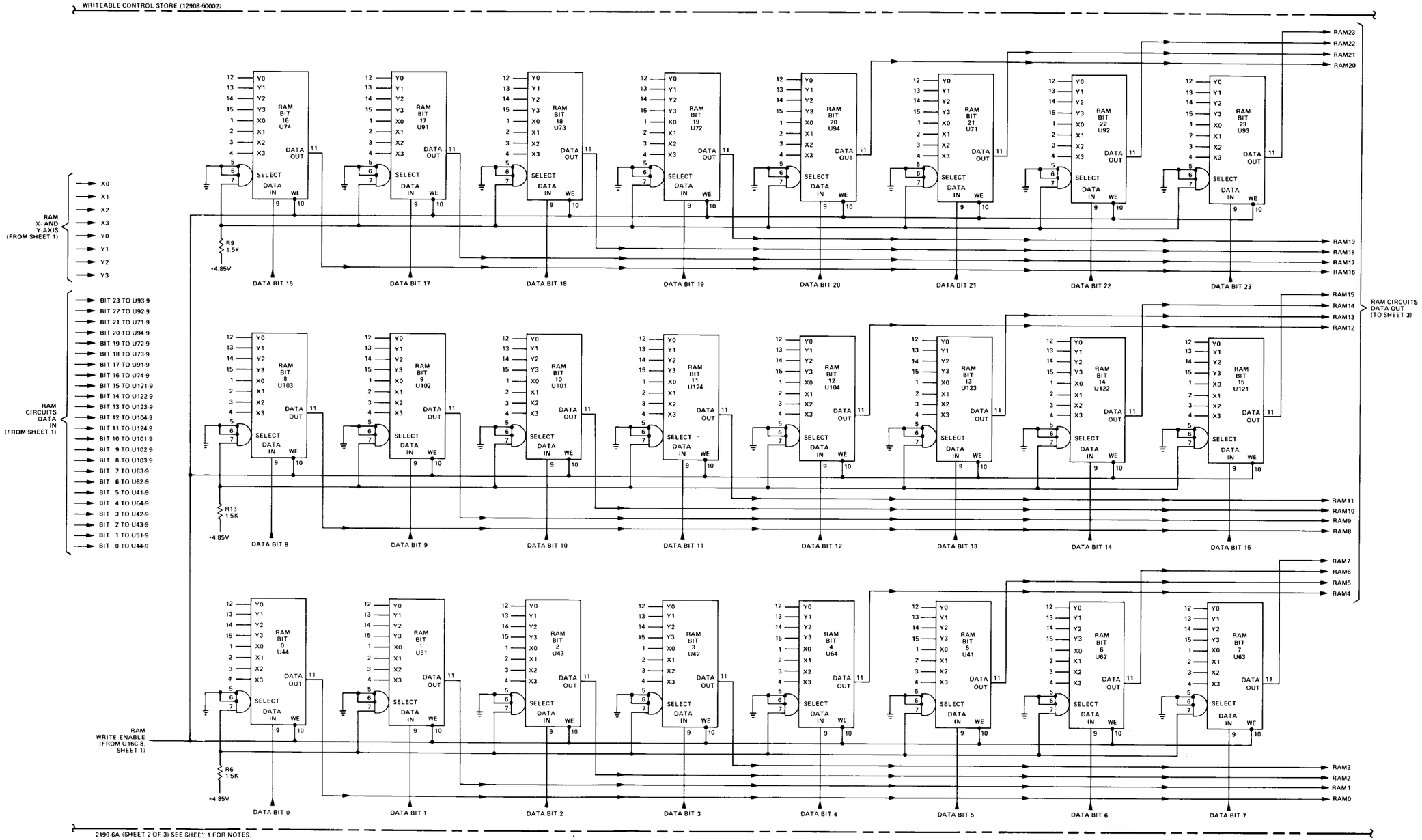


Figure 4-2. Writeable Control Store PCA, Parts Location and Schematic Diagrams (Sheet 2 of 3)

WRITEABLE CONTROL STORE (12908-60002)

RAM CIRCUITS DATA OUT (FROM SHEET 2)

RAM23 RAM22 RAM21 RAM20 RAM19 RAM18 RAM17 RAM16 RAM15 RAM14 RAM13 RAM12 RAM11 RAM10 RAM9 RAM8 RAM7 RAM6 RAM5 RAM4 RAM3 RAM2 RAM1 RAM0

(FROM SHEET 1)

DIRFF (U35A-15)

DIR FF (U35A-14)

IOI(B) (FROM U27C-11)

+4.85V

-2V

U37B U47A U47B

R1 1K R2 1K R10 215 R12 215 R2 464

U45 U55

U87A U87B U77B U77A U57B U57A U67B U67A U97B U97A U107A U107B U127B U127A U117B U117A

RAM OUTPUT BUFFER

IOB4 IOB7 IOB6 IOB1 IOB0 IOB2 IOB3 IOB5 IOB12 IOB8 IOB9 IOB10 IOB15 IOB14 IOB13 IOB11

(TO SHEET 1)

RAR9 J1-48 RAR8 J1-46 RMX J1-40 ENRMX J1-38

ROM MODULE DECODER U132

INV OUT

R16 1K +4.85V

MOD SEL S2 M3 M2 M1 M0

FROM U16A-12 (SHEET 1)

U133B U133D

S1 ON OFF WCS MOD 0

2199-68 (SHEET 3 OF 3) SEE SHEET 1 FOR NOTES.

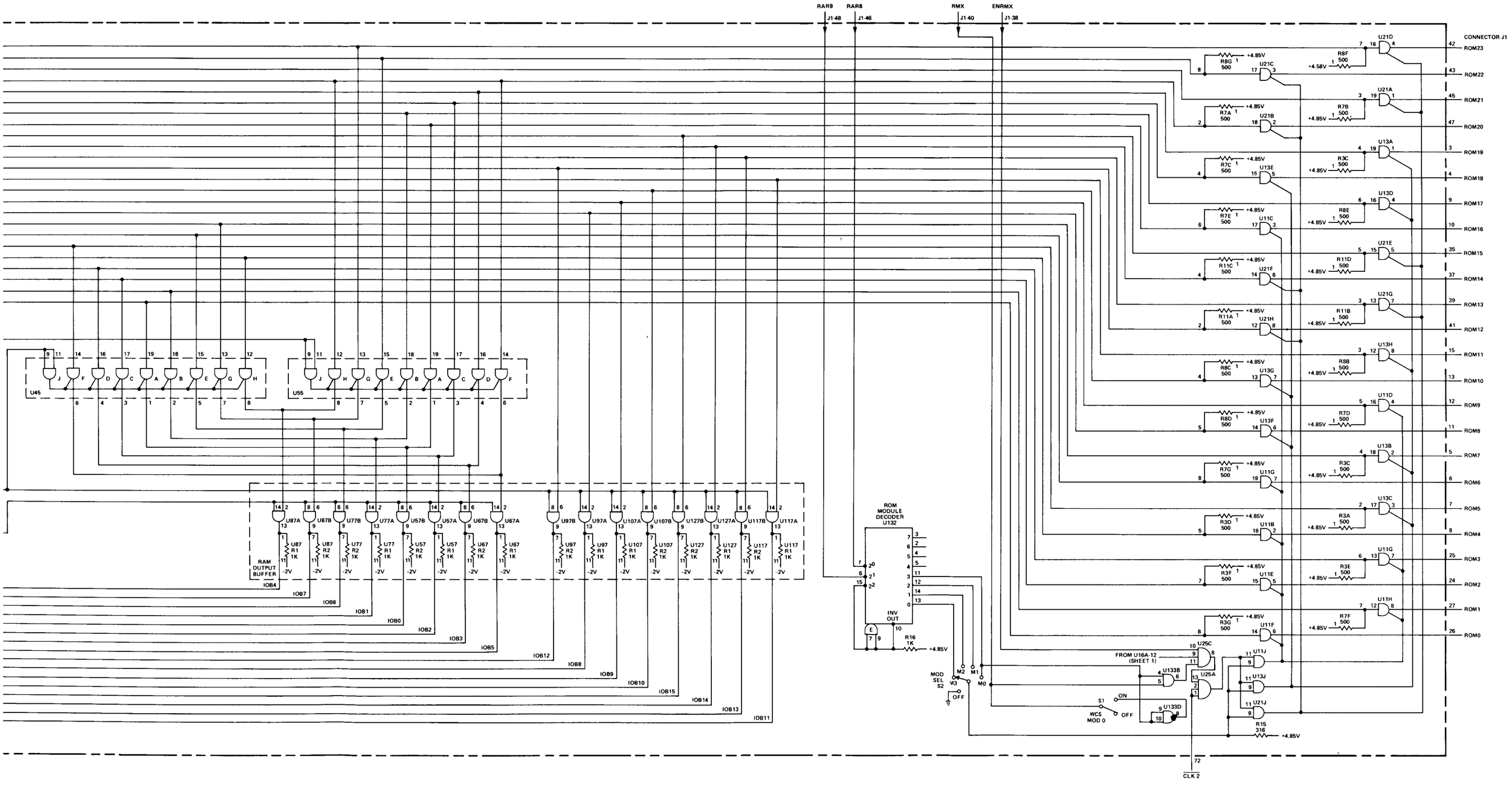


Figure 4-2. Writeable Control Store PCA, Parts Location and Schematic Diagrams (Sheet 3 of 3)

SECTION V REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section provides information for ordering replacement parts for the HP 12908A Writeable Control Store Interface Kit. Table 5-1 lists the kit parts. Table 5-2 lists parts in alphanumeric order by HP part numbers and gives the total quantity for each replaceable part in the interface kit. Table 5-3 lists the code numbers of the various manufacturers of the replaceable parts. A replaceable parts list (table 4-1) and parts location diagram (figure 4-2) for the PCA are provided in section IV of this manual.

5-3. Tables 4-1 and 5-2 provide the following information for each replaceable part:

a. Reference designation of the part (table 4-1 only). (Refer to table 5-4 for an explanation of the reference designations used in the REFERENCE DESIGNATION column.)

b. Hewlett-Packard part number.

c. Description of the part. (Refer to table 5-4 for an explanation of the abbreviations used in the DESCRIPTION column.)

d. A five-digit code identifying the manufacturer of the part. (Refer to table 5-3 for a code list of manufacturers.)

e. Manufacturer's part number.

f. Total quantity (TQ) of each part used in the kit or assembly (table 5-2 only).

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Refer to the list at the back of this manual for addresses. Specify the following information for each part ordered:

a. Identification of the kit or assembly containing the part.

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation for each part (if applicable).

Table 5-1. Writeable Control Store Interface Kit Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
12908-60002*	Writeable Control Store Interface PCA	28480	12908-60002	1
12908-60003	Writeable Control Store Jumper Board Assembly	28480	12908-60003	1
12908-60005	Backplane Jumper Assembly	28480	12908-60005	1
12908-90001	Operating and Service Manual	28480	12908-90001	1

*Option 001 consists of the PCA only.

Table 5-2. Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0150-0121	CAPACITOR, cer, 0.1 uf, -20% +80%, 50 Vdcw	13606	5C50B1-CML	7
0160-2055	CAPACITOR, cer, 0.01 uf, -20% +80%, 100 Vdcw	13606	C023F101F103ZS22-CDR	29
0160-3901	CAPACITOR, cer, 2.2 uf, ±20%, 25 Vdcw	13606	5C120-CML	7
0360-0294	TERMINAL	88245	2010B-2	7
0698-0082	RESISTOR, fxd, flm, 464 ohms 1%, 1/8W	19701	MF4CT-0	1
0698-3441	RESISTOR, fxd, flm, 215 ohms, 1%, 1/8W	19701	MF4CT-0	2
0698-3444	RESISTOR, fxd, flm, 316 ohms, 1%, 1/8W	19701	MF4CT-0	1
0757-0280	RESISTOR, fxd, flm, 1K, 1%, 1/8W	19701	MF4CT-0	4
0757-0427	RESISTOR, fxd, flm, 1.5K, 1%, 1/8W	19701	MF4CT-0	3
1810-0030	RESISTOR NETWORK, 1K, 5%, 0.15W	13606	200C1618-CRR	3
1810-0080	RESISTOR NETWORK, 500 ohms, 5%, 0.15W	13606	200 Series	4
1820-0141	IC, 74H08, quad 2 input AND gate	04713	SC7514PK	1
1820-0370	IC, 74H00, quad 2 input NAND gate	01295	SN4478	4
1820-0371	IC, 74H10, triple 3 input NAND gate	01295	SN4479	1
1820-0372	IC, 74H11, triple 3 input AND gate	01295	SN4480	1
1820-0377	IC, 74H50, dual 2-wide, 2 input AND/OR invert gate (expandable)	01295	SN4485	1
1820-0715	IC, 74H106, high speed dual edge-triggered J-K FF	01295	SN33510	1
1820-0742	IC, 9308, dual 4-bit latch FF	17803	SL17869	4
1820-0755	IC, HP147A, 8-bit driver, non-inverting	28480	1820-0755	3
1820-0759	IC, HP 106A, 8-bit receiver, non-inverting	28480	1820-0759	4
1820-0834	IC, 4038, 1 to 8 decoder w/inversion control	04713	SC18951PK	1
1820-0956	IC, 9956, dual 2 input AND buffer	17803	SL3459	10
1820-0988	IC, 93410, 256-bit read/write memory	17803	SL40850	24
3100-2687	SWITCH, SPST, 6 position, 100 ma, 28 Vdc	73138	374H	1
3101-1213	SWITCH, DPST-DB, 0.5a, 28 Vdc	81640	T8001	1
12908-60002	Writeable Control Store Interface PCA	28480	12908-60002	1
12908-60003	Writeable Control Store Jumper Board Assembly	28480	12908-60003	1
12908-60005	Backplane Jumper Assembly	28480	12908-60005	1
12908-90001	Operating and Service Manual	28480	12908-90001	1

Table 5-3. Code List of Manufacturers

Code No.	Manufacturer	Address
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
04713	Motorola Inc., Semiconductor Prod. Div.	Phoenix, Ariz.
13606	Sprague Electric Co., Transistor Div.	Concord, N.H.
17803	Fairchild Camera and Instrument Corp., Semiconductor Div.	Mountain View, Cal.
19701	Electra Mfg. Co.	Independence, Kan.
73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Cal.
81640	Control Switch Div. Control Co. of America	Folcroft, Pa.
88245	USECO Div. Litton Industries	Van Nuys, Cal.

MANUAL PART NO. 12908-90001
MICROFICHE PART NO. 12908-90006

PRINTED IN U.S.A.

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12908B

WRITEABLE CONTROL STORE INTERFACE KIT

(FOR HP 2100 COMPUTER)

Printed-Circuit Assembly:

12908-60006, Series 1309

Note

This manual should be retained with the applicable computer documentation.

Options Covered

This manual applies to option 001 as well as to the standard version of the HP 12908B Writeable Control Store Interface kit.

12908-90011

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

PRINTED: SEP 1974

CONTENTS

ILLUSTRATIONS

TABLES

SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual covers general information, installation, programming, theory of operation, maintenance and replaceable parts for the HP 12908B Writeable Control Store Interface Kit. Option 001 for the interface kit is also covered in this manual.

1-3. GENERAL DESCRIPTION.

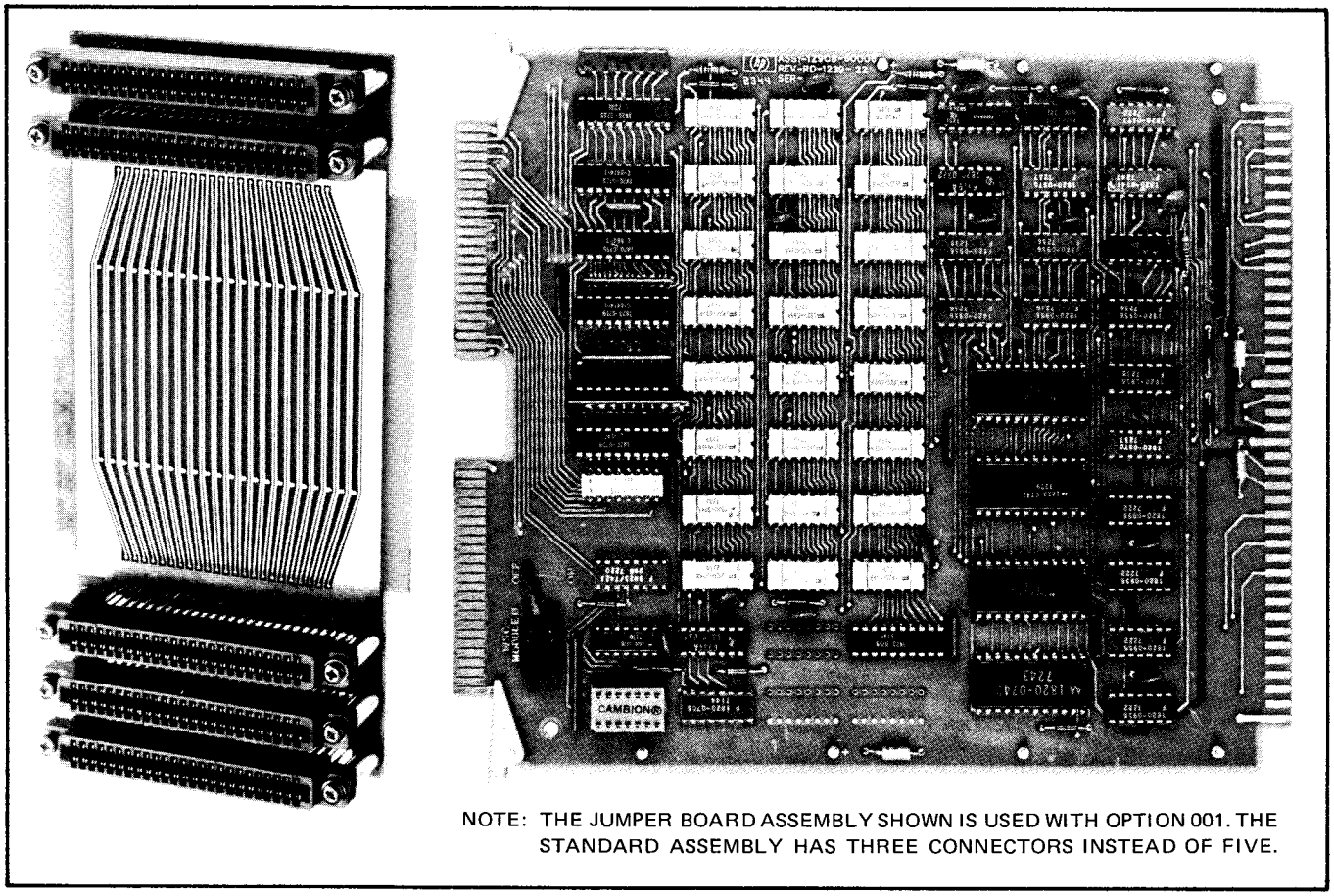
1-4. The Hewlett-Packard 12908B Writeable Control Store Interface Kit provides the HP 2100 Computer with the necessary logic to dynamically change the basic instruction set of the computer. Sections II through V of this manual provide installation and programming, theory of operation, maintenance and replaceable parts information for the kit. The printed-circuit assembly and jumper board assembly contained in the interface kits are shown in figure 1-1 and listed in table 1-1.

1-5. IDENTIFICATION.

1-6. Hewlett-Packard uses five digits and a letter (00000A) for standard kit designations. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office. These offices are listed at the back of this manual.

Table 1-1. Interface Kit Contents

INTERFACE KIT	CONTENTS	HP PART NO.
12908B	Writeable Control Store PCA	12908-60006
	Jumper Board Assembly	12908-60008
	Operating and Service Manual	12908-90011
12908B-001	Writeable Control Store PCA	12908-60006
	Jumper Board Assembly	12908-60003



NOTE: THE JUMPER BOARD ASSEMBLY SHOWN IS USED WITH OPTION 001. THE STANDARD ASSEMBLY HAS THREE CONNECTORS INSTEAD OF FIVE.

2262-1

Figure 1-1. Writeable Control Store Interface Kit

1-7. Printed-circuit assembly (PCA) revisions are identified by a letter, a series code, and a division code stamped on the board (e.g., A-1152-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the logic diagram in this manual, there are differences between your PCA and the PCA described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

1-8. Manuals and manual supplements are identified by title and part number on the title page of the doucment.

1-9. OPTIONS.

1-10. Option 001 provides additional writeable control store to the basic kit. This option consists of one writeable control store PCA and the optional jumper board assembly; specify quantity (up to two per system) when ordering. Also note that it is necessary to have the basic kit before option 001 can be used in the system.

1-11. SPECIFICATIONS.

1-12. Table 1-2 lists the characteristics and specifications of the writeable control store PCA.

Table 1-2. Writeable Control Store PCA Specifications

CAPACITY

Words Available: 256 per module
Maximum WCS Modules: 3 per HP 2100
Word Size: 24-bits
Maximum Primary Entry Points: 16

MICROINSTRUCTION TIME

196 nanoseconds

INSTALLATION

One writeable control store PCA requires the use of one Input/Output slot (slot 10). Option 001 requires the use of three Input/Output slots (slots 10, 11, and 12, inclusive). Writeable control store may be used as any module. Module 1, 2 or 3 is normally used. Also available but not recommended by Hewlett-Packard is Module 0, which contains the basic HP 2100 Computer instruction set).

DATA STORAGE

Input/Output Group instructions or via an HP 2100 Direct Memory Access channel (if present).

DATA READBACK

Input/Output Group instructions only.

INTERFACE CURRENT SUPPLIED BY COMPUTER

0.15V (-2V supply); 4.6A (+4.85V supply)

PCA DIMENSIONS

Width: 7-3/4 inches (196.8 mm)
Height: 8-11/16 inches (220.7 mm)

PCA WEIGHT

Net Weight: 18 oz (511.2 gm) (card and cable only)
Shipping Weight: 4 lb (2.27 kg)

PCA INPUT LEVELS

"1" state: 1.9 volts min.
"0" state: 1.1 volts max.

PCA OUTPUT LEVELS

"1" state: 2.4 volts min.
"0" state: 0.7 volt max.

2-1. INTRODUCTION.

2-2. This section provides procedures and information for unpacking and inspection, installation, programming, and reshipment of the writeable control store kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracked, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged item without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. Install the writeable control store kit as follows:

a. Ensure that the computer operates properly prior to installing the writeable control store interface kit.

b. Turn off power at the computer.

c. Remove the top and bottom access covers from the computer. Then remove and discard the front plastic strip from the strengthener on the underside of the top access cover.

d. Remove timing and control PCA A1, part no. 02100-60014, from slot 1 of the computer and verify that the revision data is not A-1116-22. If the revision data is A-1116-22, locate the printed circuit traces connected to pins 38 and 40 of 50-pin connector J1. Cut these traces with a sharp knife so that no electrical contact is made to these pins.*(See CAUTION.)* This action does not affect the operation of the computer in any way. Replace the timing and control PCA in slot 1.

CAUTION

PCA A1 is a multilayer board and can be easily damaged if the traces are carelessly cut.

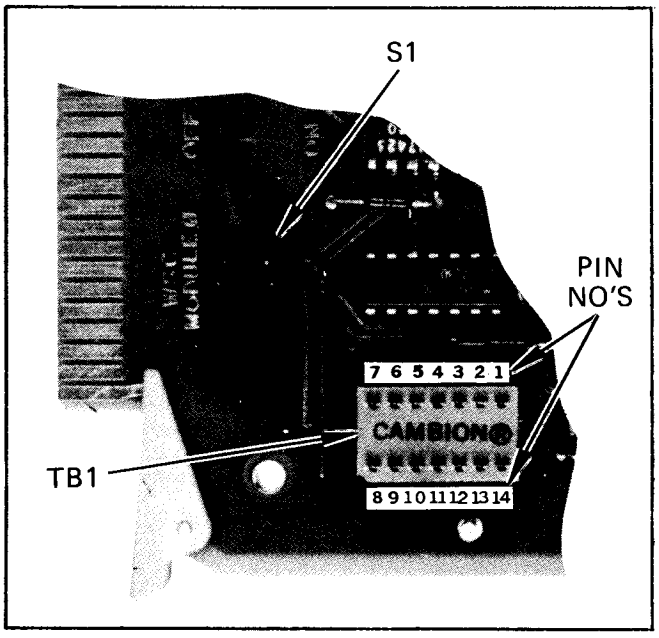
e. Remove ROM control PCA A2, part no. 02100-60002, from slot 2 of the computer. Refer to table 2-1 and configure jumpers W1 through W6 to the desired number of modules.

Table 2-1. ROM Control PCA A2 Jumper Connections for Various Module Configurations

MODULES INSTALLED (INCLUDING ROM MODULES)	JUMPERS TO BE INSTALLED					
	W1	W2	W3	W4	W5	W6
0	A to B	D to K	E to F	in	out	H to L
0, 1	A to B	none	none	in	out	H to L
0, 2	none	D to K	E to F	out	in	none
0, 3	A to B	C to D	E to F	in	in	G to H
0, 1, 2	A to D	none	E to F	in	out	none
0, 1, 3	A to B	none	none	in	out	G to H
0, 2, 3	none	C to D	E to F	out	in	none
0, 1, 2, 3	none	none	none	in	out	none

f. Replace ROM control PCA A2 in slot 2.

g. On the writeable control store PCA (or PCAs, if installing option 001), to select the desired module number position remove the appropriate jumper wires from TB1 (see figure 2-1 for pin number configuration). Refer to table 2-2 for desired module number and jumper removal.



2262-2

Figure 2-1. WCS Terminal Board for Selecting Module Number Position

Table 2-2. WCS PCA Jumper Removal on Terminal Board for Various Module Selections

MODULE	JUMPERS TO BE REMOVED
0	NONE
1	Pins 6, 9
2	Pins 5, 10
3	Pins 5, 10, 6, 9

h. On the writeable control store PCA, place WCS module 0 enable switch S1 in the OFF position.

i. Place the first writeable control store PCA in slot number 10 (select code 25) of the I/O section of the computer. Any additional writeable control store PCAs should be placed in slots 11 and 12 for select codes 24 and 23, respectively, in that order.

Note: If an I/O extender card, part no. 02155-60003, previously occupied slot 10, it must now be installed in slot 11. For option 001, the I/O extender card must be installed in slot 13 and device I/O cards previously occupying slots 11 and 12 must now be installed in the HP 2155A Input/Output Extender. Software must be reconfigured as required to reflect new select code of I/O extender and, if necessary, device I/O cards relocated in HP 2155A. Also, an I/O jumper board, part no. 02116-6110 must be placed in the first slot (select code 25) of the I/O extender.

j. Install the jumper board assembly, part no. 12908-60008, (12908-60003 for option 001) on connector J1 of the writeable control store PCA, connector J1 of ROM control PCA A2, and connector J1 of timing and control PCA A1. (Connector J1 is the connector closest to the front of the computer.)

k. Replace the top and bottom access covers on the computer.

l. Turn on power at the computer and perform the diagnostic test as outlined in the Diagnostic Program Procedures (part no. 12908-90013) contained in the *Manual of Diagnostics.* If the diagnostic program is completed without error, the card is installed and operating properly. If the diagnostic program indicates errors, halt the computer, turn off power and recheck all of the above installation procedures (correct where necessary), then recheck and repeat the operating procedures of the diagnostic.

2-7. RESHIPMENT.

2-8. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-9. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-10. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 Cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N. J. and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note: In any correspondence, identify the kit by model number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-11. PROGRAMMING.

2-12. Two methods exist for writing data into (loading) a writeable control store module: under program control, and via DMA (if available). Under program control, prior to initiating the load routine, the data to be loaded must be stored in the computer memory. This will require a block of up to 512 words per module. The load routine will send two words from memory (32 bits which are mapped into an 8-bit address and a 24-bit microinstruction) to the writeable control store module, issue a write command to that module and cause the data to be stored there. The load routine will repeat this process until the desired number of words have been stored in the writeable control store module.

2-13. Once loaded, the contents of the writeable control store module may be read back under program control via the I/O bus and compared with its counterpart in memory.

2-14. The following is an example of the program sequence necessary for loading writeable control store under program control. This example does not include block pointers, counters, etc., which are necessary for proper control.

Note: "sc" indicates select code of WCS PCA.

STF	sc	Initializes the Direction FF.
OTA	sc	Loads first computer word into first WCS buffer and toggles the Direction FF. This word comprises the eight-bit address and the eight most significant bits of the microinstruction.

OTB	sc	Loads the second computer word into the second WCS buffer and toggles the Direction FF. This word comprises the 16 least significant bits of the microinstruction.
STC	sc	Provides the write pulse to load the WCS buffers into the RAM.

2-15. The OTA, OTB, and STC instructions are normally in a loop that is repeated until the desired number of microinstructions have been stored. OTA/OTB was chosen as an example, any combination of these instructions is allowable.

2-16. An example of reading from writeable control store under program control via the I/O bus is shown below. This example is shown without regard to the block pointers, counters, etc., which are necessary for proper control.

Note: "sc" indicates the select code of the WCS PCA.

STF	sc	Initializes the Direction FF.
OTA	sc	Sends the eight-bit address to the WCS module from the eight most significant bits of the A-register. (B-register could be used.)
STF	sc	Re-initializes the Direction FF.
LIA	sc	Places eight zeros into the eight most significant bit positions of the A-register and places the eight most significant bits of the microinstruction into the eight least significant bit positions of the A-register.
LIB	sc	Places the 16 least significant bits of the microinstruction into the B-register.

2-17. The STF, OTA, STF, LIA, and LIB sequence is normally in a loop that is repeated until the desired number of microinstructions have been read in from writeable control store. LIA/LIB was chosen as an example, any combination of these instructions is allowable.

2-18. Under DMA control, the load routine must send only the three DMA control words to the selected channel. When the channel is turned on, DMA will utilize every memory cycle until the entire block of data is sent to the writeable control store module (maximum of 512 cycles). DMA will transfer these words at a rate of 980 ns/word (512 words will take 502 μs to transfer).

2-19. The following is an example of the program sequence necessary for loading writeable control store via DMA. This example does not include block pointers, counters, etc, which are necessary for proper control.

Note: "sc" indicates the select code of the WCS PCA.

LDA	CW1	Get the first DMA control word.
OTA	6	Send the first DMA control word to the selected DMA channel. (DMA channel 1 has been selected here for demonstration purposes only.)
CLC	2	Prepare the selected DMA channel to receive the second DMA control word.
LDA	CW2	Get the second DMA control word.
OTA	2	Send the second DMA control word to the selected DMA channel.
STC	2	Prepare the selected DMA channel to receive the third DMA control word.
LDA	CW3	Get the third DMA control word.
OTA	2	Send the third DMA control word to the selected DMA channel.
STC	6,C	Turn on the selected DMA channel.
STF	sc	Initialize the Direction FF.
CLF	sc	Start the DMA transfer.
SFS	6	Test for the completion of the transfer.
JMP	*-1	Loop until done.
CW1	OCT	12000sc
CW2	OCT	Starting address of the block to be transferred.
CW3	OCT	Two's complement of the number of computer words to be transferred.

SECTION III THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section presents the theory of operation of writeable control store within the HP 2100 Computer. A logic diagram, parts location diagram and replaceable parts list are located in section IV of this manual.

3-3. WRITEABLE CONTROL STORE OPERATION.

3-4. Writeable Control Store (WCS) consists of a bipolar semiconductor Random Access Memory (RAM) containing 24 integrated circuit (IC) packages mounted on a 2100-size printed-circuit assembly. Also included is the jumper board assembly necessary for complete mechanization within the HP 2100 Computer. The WCS printed-circuit assembly can be installed only in slot 10 (standard) and 11 or 12 (option 001) of the computer I/O slots. Each IC package is configured in 256 bits organized as one bit per word. Thus one module of WCS is capable of storing 256 words of 24 bits each. Up to three modules of WCS may be installed in a HP 2100 Computer.

3-5. For proper addressing of WCS, an integrated circuit comparator and terminal board (with jumpers) on the WCS PCA is used to identify that PCA as a particular module of control store (module 1, 2, or 3). For example, if the terminal board is configured for module 2, (described in step g of paragraph 2-5), the PCA will be enabled when the ROM Address Register (RAR) contains the pattern "10" in its two most significant bits (bits 9 and 8), and disabled otherwise. When enabled, the word in WCS addressed by RAR bits 0 through 7 will be sent to the ROM Instruction Register (RIR) as signals ROM0 through ROM23. The computer will then execute this word (microinstruction) as though it came from the basic computer instruction set in the control store on ROM control PCA A2 (module 0). The access time of data from WCS (140 ns) allows the computer to operate at its normal clock rate (196 ns). If it is desired to operate WCS as module 0, the WCS module 0 switch (S1) on the WCS PCA must be set to the ON position (see note following) and all jumpers restored on TB1. This enables WCS as module 0 and inhibits the control store module 0 on ROM control PCA A2. If the computer contains a module in ROM other than module 0 (for example, if floating point is installed as module 1 on the ROM control PCA) and it is desired to operate WCS as the module, the ROM integrated circuits must be removed from the ROM control PCA in order to prevent unwanted "or" conditions of the data lines (ROM0 through ROM23).

Note: Switch S1 must be set to the OFF position while WCS is being loaded. The computer must be halted following the load, at which time switch S1 is set to the ON position. The computer may then be operated using the WCS module 0 as its basic control store.

3-6. WCS also consists of the software which allows it to be used as a dynamically microprogrammed control store for the HP 2100 Computer. This software includes an assembler for converting the microcode to machine code, a driver to load the machine code into WCS and verify the load, and a mask generator to produce the tapes necessary to produce ROMs, if desired. An operating system is also provided for altering the contents of WCS during the debug phase.

3-7. The WCS PCA plugs into any of the I/O slots of the HP 2100 Computer (slots 10, 11, and 12 are recommended; see paragraph 2-6) and can be used as a replacement for, or an extension of the existing ROM control store. Up to three PCAs may be used per computer to give a maximum of 768 by 24 bits of WCS words.

3-8. Writeable control store is connected to the computer central processor through the I/O structure (for loading and checking), and also through a 50-wire PCA connector. It is this connector that enables writeable control store to be used as an extension of the computer's basic control store. The cable connects one or more (maximum of three) writeable control store PCAs to ROM control PCA A2 and timing and control PCA A1. The ROM address register on PCA A2 sends a 10-bit address to the writeable control store PCA or PCAs through this cable, and the addressed PCA then sends its data (microinstruction) from that address back through the cable. The cable is terminated on PCA A2 where the 24 data lines (ROM0 through ROM23 are "or" tied onto the corresponding outputs of the basic control store. From there the data is sent to the ROM instruction register as though it was from the basic control store.

3-9. For the purpose of execution of WCS instructions, WCS can be configured to be addressed as any one of the computer's four ROM modules including module 0. However, when configured as module 0, the basic ROM module 0 is disabled.

3-10. To load the WCS RAM circuits, the WCS PCA must be addressed through the I/O interfacing structure of the computer. A 32-bit format is necessary, requiring that a 2-word transfer through the machine A and/or B registers be used in the loading procedure. Two computer words and thus two transfer operations are required for one WCS word. The eight most significant bits of the first computer word transferred is the WCS RAM circuit address where the remaining

eight bits of the first computer word and all 16 bits of the second computer word (total 24 bits) will be stored.

3-11. Once loaded, WCS becomes an extension of the ROM via the ROM control PCA. Thus the WCS may be used to alter the computer instruction set while the computer is in an operating condition. This feature permits dynamic expansion of the computer instruction set.

3-12. DETAILED THEORY.

3-13. COMPUTER POWER ON.

3-14. When power is initially applied by the POWER switch on the computer, the POPIO signal is applied at time T5 to the WCS PCA at pin 17. This signal causes the SRQ FF to clear and the DIR FF to set.

3-15. LOADING OPERATION.

3-16. To explain the loading operation of WCS, use will be made of the loading program described in section II of this manual, the WCS loading timing diagram (figure 3-1), and the schematic diagram (figure 4-2).

3-17. The first instruction of the program is the STF instruction. This instruction causes the signal STF to be generated at time T3 and applied to pin 9 of the WCS PCA. This signal, along with the proper select code, causes the SRQ FF to clear and the DIR FF to set. The first output instruction is then issued, generating the signal IOO. Signal IOO is applied to pin 20 of the WCS PCA and it, along with the proper select code, causes the data on the IOB lines (first computer word to be transferred) to be gated into the RAM address register and the eight most significant bits of the RAM data register. The IOO signal also causes the TGL FF to be set at time T3, which causes the DIR FF to be cleared as soon as signal IOO goes low at time T5. The second output instruction again causes signal IOO to be generated, gating the second computer word into the 16 least significant bits of the RAM data register. This second IOO signal again sets the TGL FF at time T3 causing the DIR FF to be set. The STC instruction causes the signal STC to be generated, setting the CTL FF and gating the 24 bits of data in the WCS data register into the addressed WCS RAM location at time T5. This one location in the WCS RAM is loaded with 24 bits from the computer.

3-18. CHECKING OPERATION.

3-19. The checking operation of WCS is essentially the same as the loading operation except that the signal IOI is generated by the two output instructions, causing the DIR FF to be toggled and RAM bits 0 through 24 to be gated at the appropriate times onto the IOB lines.

3-20. DMA OPERATION.

3-21. The direct memory access (DMA) function of the computer provides a direct data path between the computer memory and writeable control store (WCS) via software selection. During a DMA data transfer, the central processor is disabled and the DMA circuits supply the required control signals to operate the memory and WCS. Consecutive memory cycles can be utilized by DMA, allowing a maximum data transfer rate of one million words per second. DMA data transfers are accomplished in blocks, with the block length specified by software. Maximum block length for WCS is 512 computer words. The DMA circuits can be programmed to interrupt at the end of a data block transfer to a subroutine to re-initialize DMA for another data block transfer facilitating the successive loading of successive WCS modules.

3-22. DMA INITIALIZATION. Three control words are used to initialize a DMA channel. The control words are briefly described as follows:

a. Control Word 1 (CW1). Specifies the select code of the I/O device to provide or receive data (bits 0 through 5) and if CLC (bit 13) or STC (bit 15) signals are to be provided to the I/O interface after each word transfer.

b. Control Word 2 (CW2). Specifies input or output DMA operation (bit 15) and the starting address in memory (bits 0 through 14) of the data block.

c. Control Word 3 (CW3). Specifies the length of the data block (bits 0 through 15) and is expressed in two's-complement form.

3-23. All three control words are transferred to the DMA circuits via the S-bus.

3-24. Control Word 1 is loaded into the DMA service select register, CLC Select FF, and STC Select FF by an OTA 06 instruction. Control words 2 and 3 are both loaded into their respective registers by an OTA 02 instruction. A programmed CLC 02 clears the register load control and enables the S-bus data to the memory address register and the In/Out Select FF. An OTA 02 instruction with Control Word 2 in the computer A-register then transfers the control word to its respective registers. Prior to transferring Control Word 3, an STC 02 instruction sets the register load control and enables the S-bus data to the word count register. Another OTA 02 instruction with Control Word 3 in the computer A-register transfers the two's complement of the data block length to the word count register.

3-25. The last step to initialize the DMA circuits is accomplished by an STC 06 instruction. This sets the DMA Control FF and the Transfer Enable FF. The Control FF in the set state enables the DMA interrupt logic and must be cleared by a CLC 06 instruction if an interrupt at the end of a data block transfer is not desired. The Transfer Enable FF in the set state enables the set input to the Cycle Request FF.

3-26. The channel-one DMA circuits are now initialized and a service request from WCS will initiate the first DMA cycle. Channel-two initialization is identical except for the select codes used to address the channel. For initialization of channel-two, select code 03 replaces select code 02 and select code 07 replaces select code 06.

3-27. The DMA cycle is initiated when WCS, with a true SRQ signal, that it is ready for data transfer. The SRQ

selector provides a true Service Request to the Cycle Request FF. The Cycle Request FF is clocked to the set-state by the leading edge of SIR signal at T5 and the PH5 FF is clocked to the set-state by the trailing edge of the SIR signal (at the beginning of T6). The SPH5 signal to the control section causes the central processor to freeze at I/O time T6 to prevent further processing of programmed instructions until the DMA cycle is complete. The DMA cycle begins at T6 and continues until the PH5 FF is cleared at the next time T6. At T6 during the DMA cycle, the memory address register output is strobed onto the S-bus and at the end of this time T6, the memory address register and the word count register are incremented for the next DMA cycle.

3-28. Control signals generated by the DMA circuits perform the following operations during a DMA output operation:

a. Signal RW, at time T6, initiates a memory section read-write cycle to begin at time T2.

b. Combined true STORE and SELM signals, at time T6, load the S-bus data into the memory section M-register.

c. Combined true READ and SELT signals, at time T4T5, transfer memory section T-register data to the S-bus.

d. Signal SIOB, at time T4T5, transfers the S-bus data, via the I/O-bus, to the WCS address and data registers.

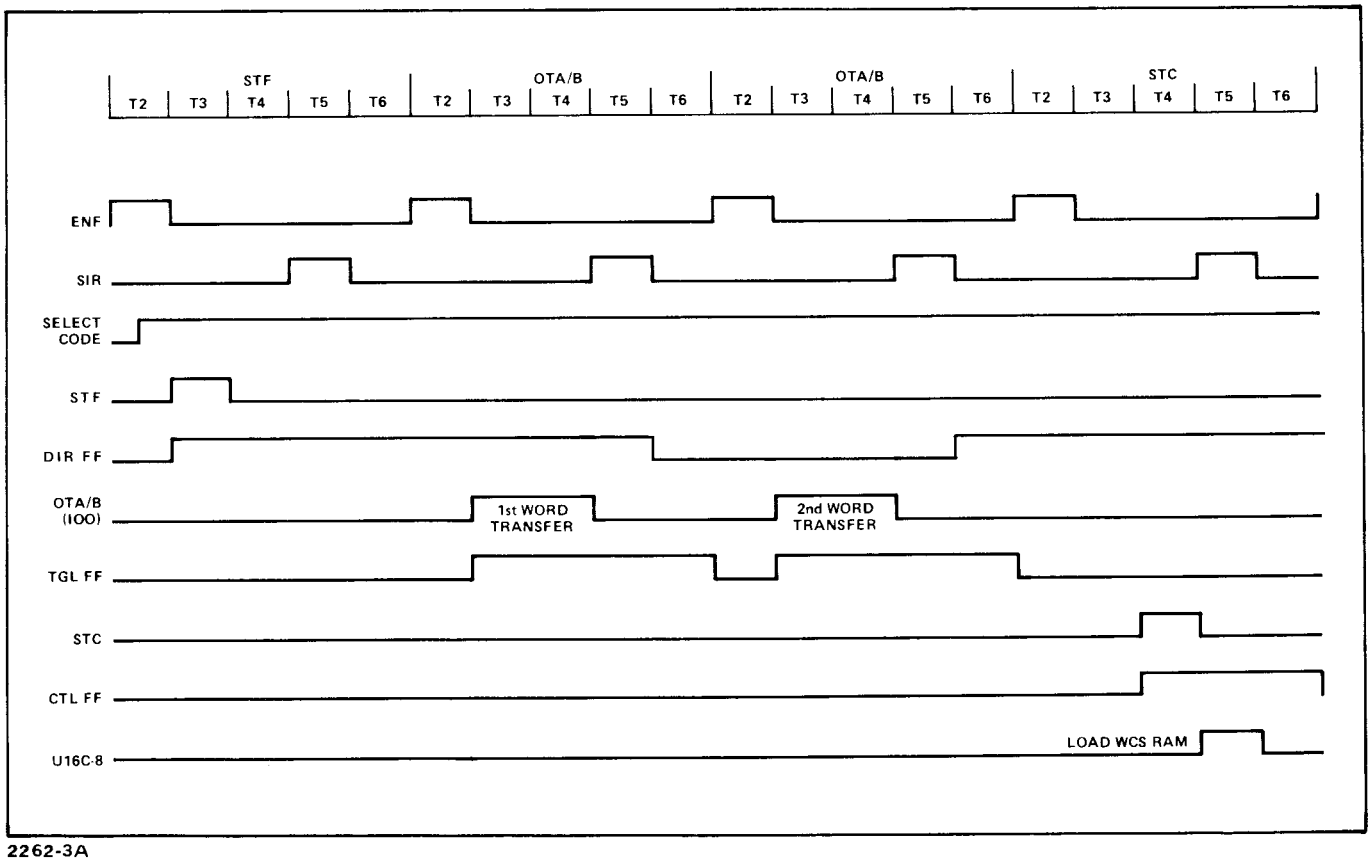
e. Signal CLF, at time T3 ensures that the WCS SRQ signal will remain true to guarantee that WCS will steal the next cycle. This allows the 1-MHz transfer rate.

f. Signal STC, at time T3, if selected, signals WCS to accept data.

3-29. END DATA TRANSFER. As stated, the word count register is loaded with the two's complement of the data block length. The word count register is incremented every DMA cycle so that during the last cycle of the data block, a carry is generated out of the last stage (bit 15) of the word count register. This carry, designated Word Count Rollover (WCR), clears the Transfer Enable FF and sets the Flag Buffer FF. The Transfer Enable FF, in the clear state, inhibits any further service requests to the Cycle Request FF. The Flag Buffer FF, in the set state, initiates the DMA interrupt logic.

3-30. At time T2 during the last DMA cycle, the Flag FF sets; if the Control FF is set, the IRQ FF sets at time T5. Signals FLG and IRQ from the IRQ FF initiate an I/O interrupt to the DMA channel interrupt address (00006 or 00007). A DMA interrupt service routine may then be used to re-initialize the DMA channel for another data block transfer.

3-31. With a CLC in control word one, the roll-over will also force DMA to issue a CLC to WCS, thereby clearing the SRQ FF.



2262-3A

Figure 3-1. WCS Loading Timing Diagram

4-1. INTRODUCTION.

4-2. This section contains information on diagnostics and troubleshooting for the writeable control store kit.

4-3. PREVENTIVE MAINTENANCE.

4-4. Preventive maintenance for the writeable control store kit should be performed when the preventive maintenance routines for the computer system are performed. Preventive maintenance consists of inspecting the writeable control store PCA and jumper board assembly for burned or broken components, loose connections, and deteriorated insulating materials.

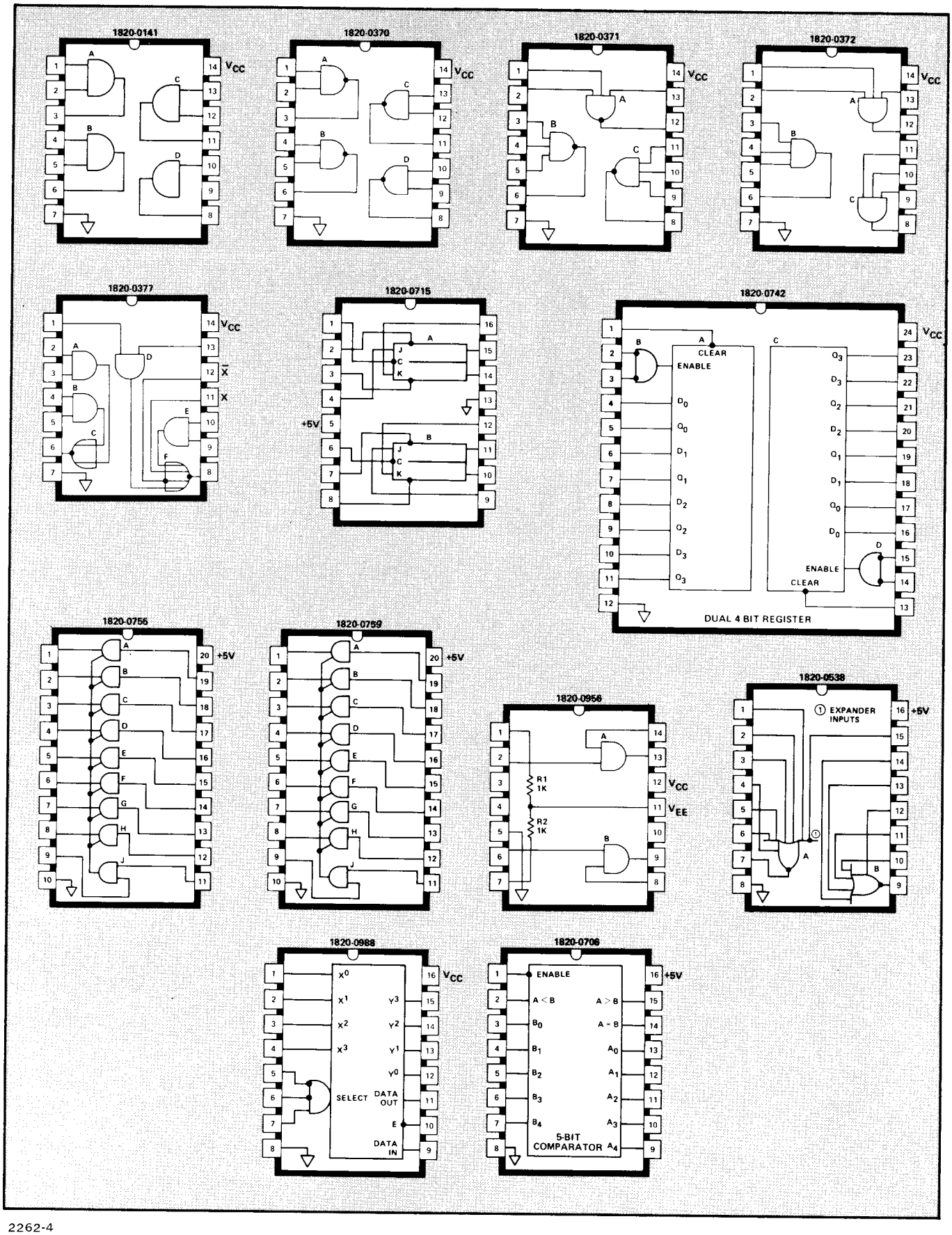
4-5. TROUBLESHOOTING.

4-6. Troubleshooting for the writeable control store interface kit is accomplished by performing the tests in the diagnostic program and analyzing any error messages that occur as the test is being run. Paragraph 1-4 lists the items that make up the writeable control store interface kit. Table 4-1 contains a replaceable parts list for the writeable control store PCA with parts listed in alphanumeric order by reference designation. Figure 4-1 illustrates the internal layout of the integrated circuits used in this kit. Figure 4-2 contains a logic diagram and parts location diagram of the writeable control store PCA.

Note: If it is necessary to extend the WCS PCA from the computer for troubleshooting purposes, two extender PCA's, part no. 02116-63216, are necessary. One extender is used to extend the WCS PCA and one extender is used to extend ROM control PCA A2.

Table 4-1. Writeable Control Store PCA, Replaceable Parts

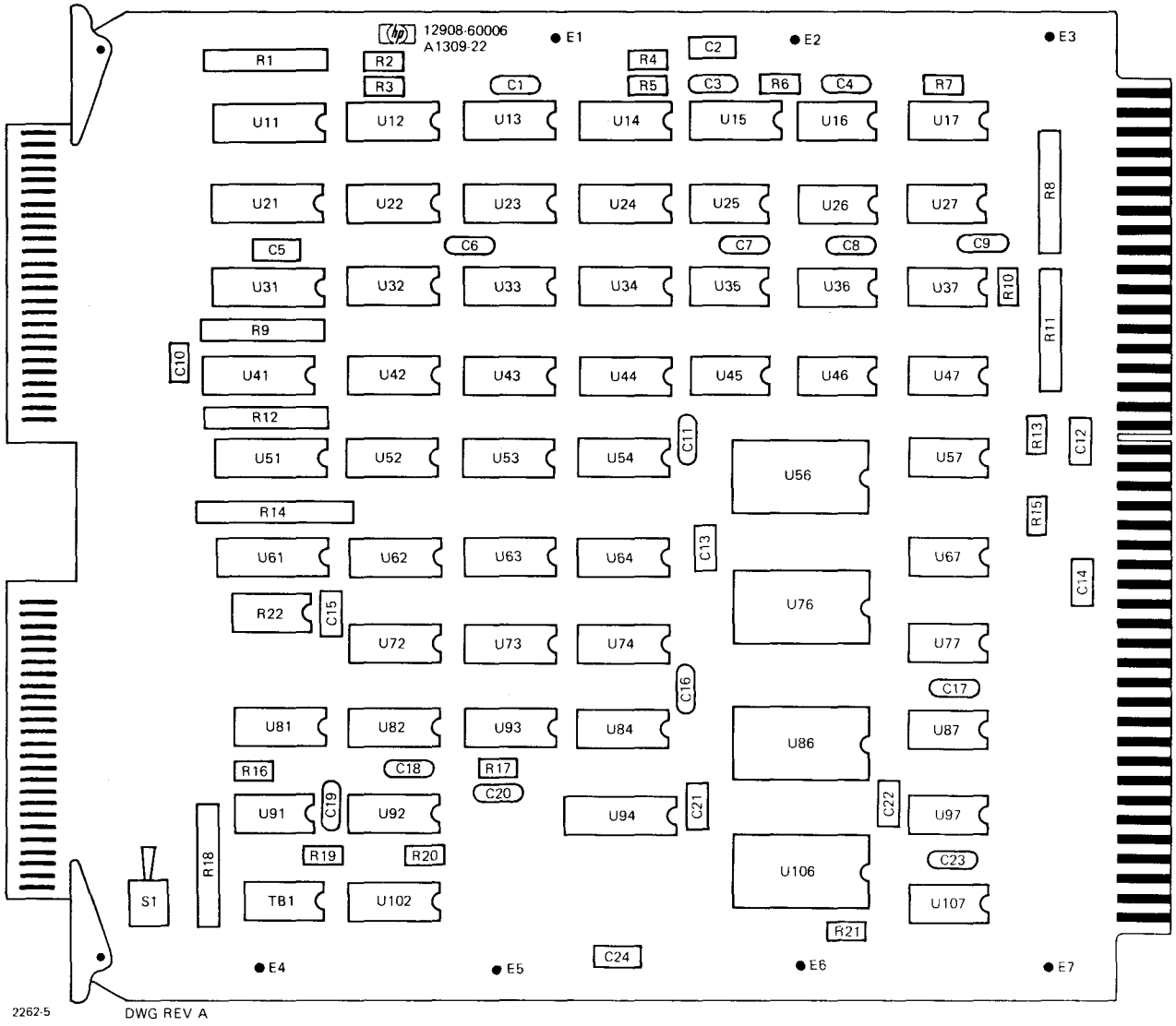
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,3,4,6 thru 9, 11,16 thru 20,23	0160-2055	CAPACITOR, Cer, 0.01 µf, -20% + 80%, 100 Vdcw	13606	C023F101F103ZS22-CDR
C2,12,14,24	0180-0197	CAPACITOR, fxd, elect, 2.2 µf, ±10%, 20 Vdcw	56289	150D225X9020A2-DYS
C5,10,13,15,21,22	0150-0121	CAPACITOR, Cer, 0.1 µf, -20% + 80%, 50 Vdcw	13606	5C50B1-CML
E1 thru 7	0360-0294	TERMINAL	88245	2010B-2
R1,9,12	1810-0080	RESISTOR NETWORK, 500 ohms, 5%, 0.15W	13606	200 Series
R2,4,10	0698-5852	RESISTOR, fxd, flm, 500 ohms, 1%, 1/8W	28480	0698-5852
R3,5,17	0757-0427	RESISTOR, fxd, flm, 1.5K, 1%, 1/8W	19701	MF4CT-0
R6,16,19,21	0757-0280	RESISTOR, fxd, flm, 1K, 1%, 1/8W	19701	MF4CT-0
R7	0698-0082	RESISTOR, fxd, flm, 464 ohms, 1%, 1/8W	28480	0698-0082
R8,11,18	1810-0030	RESISTOR NETWORK, 1K, 5%, 0.15W	13606	200C1618-CRR
R13,15	0698-3441	RESISTOR, fxd, flm, 215 ohms, 1%, 1/8W	19701	MF4CT-0
R14	1810-0055	RESISTOR NETWORK, 10K, 5%, 0.125W	28480	1810-0055
R20	0757-0438	RESISTOR, fxd, flm, 5110 ohms, 1%, 1/8W	28480	0757-0438
R22	1810-0037	RESISTOR ARRAY, cermet, 1K, 2%, 1-3/4W per array	28480	1810-0037
S1	3101-1213	SWITCH, DPST-DB, 0.5a, 28 Vdc	81640	T8001
TB1	5060-8342	JUMPER ASSEMBLY, PCA	28480	5060-8342
U11,31,51	1820-0755	INTEGRATED CIRCUIT, TTL, 8-bit driver, non-inverting	28480	1820-0755
U12,13,14,22,23,24, 32,33,34,42,43,44, 52,53,54,62,63,64, 72,73,74,82,83,84	1820-0988	INTEGRATED CIRCUIT, TTL, 256-bit read/write memory	17083	SL40850
U15	1820-0715	INTEGRATED CIRCUIT, TTL, high speed dual edge-triggered J-K FF	01295	SN33510
U16	1820-0371	INTEGRATED CIRCUIT, TTL, triple 3-input NAND gate	01295	SN4479
U17	1820-0377	INTEGRATED CIRCUIT, TTL, dual 2-wide, 2-input AND/OR invert gate (expandable)	01295	SN4485
U21,41,61,94	1820-0759	INTEGRATED CIRCUIT, TTL, 8-bit receiver, non-inverting	28480	1820-0759
U25,92	1820-0372	INTEGRATED CIRCUIT, TTL, triple 3-input AND gate	01295	SN4480
U26,37,67,91	1820-0370	INTEGRATED CIRCUIT, TTL, quad 2-input NAND gate	01295	SN4478
U27	1820-0141	INTEGRATED CIRCUIT, TTL, quad 2-input AND gate	04713	SC7514PK
U35,36,45,46,47,57, 77,87,97,107	1820-0956	INTEGRATED CIRCUIT, CTL, dual 2-input AND buffer	17803	SL3459
U56,76,86,106	1820-0742	INTEGRATED CIRCUIT, TTL, dual 4-bit latch FF	17803	SL17869
U81	1820-0538	INTEGRATED CIRCUIT, TTL, dual 4-input NAND gate	28480	1820-0538
U102	1820-0706	INTEGRATED CIRCUIT, TTL, 5-bit comparator	28480	1820-0706
X1	1200-0474	SOCKET, INTEGRATED CIRCUIT, 14 pin	28480	1200-0474



2262-4

Figure 4-1. Integrated Circuit Diagrams

12908B


12908-60006
A1309-22
E1
E2
E3
E4
E5
E6
E7
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
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U72
U73
U74
U76
U77
U81
U82
U93
U84
U86
U87
U91
U92
U94
U97
U102
U106
U107
TB1
S1
2262-5
DWG REV A

WRITEABLE CONTROL STORE (12908-60006, SERIES 1309)

ADDRESS BUFFER U61

RAR0 J1-33 · RAR1 J1-31 · RAR2 J1-29 · RAR3 J1-23 · RAR4 J1-22 · RAR5 J1-21 · RAR6 J1-19 · RAR7 J1-17

R22 1K · R14 10K

-2V 47,48 · GND 1,2 85,86 · +4.85V 39,40

C10,C24 C40 2.2 (3)

C1,C21 C32,C43 2.2 (4)

C2,C3,C6,C7, C11,C12,C14, C16-C20,C22, C23,C25-C31, C33-C39 0.01 (29)

C4,C5,C8, C9,C13, C15,C41 0.1 (7)

SCM 14 · SCL 16 · IOG 15 · STC 22

U25B

R8A 1K · R8B 1K · R8C 1K · R11C 1K

ENF 46 · SIR 32

R11F 1K · R11G 1K

IOO 20 · R11A 1K

IOI 24 · R11E 1K

STF 9 · R8E 1K

POPIO 17 · R8F 1K

CLC · R11D 1K

CLF 7 · R83 1K

U26 · U27 · U67 · U47

CONTROL FF U37

TOGGLE FF U37

U17 (NC)

SRQ FF U16

U16A · U16C

RAM WRITE ENABLE (TO SHEET 2)

DIR FF U15

H6 1K · +4.85

R11B 1K

R21 1K · +4.85V

ADDRESS BUFFER U94

RAM ADDRESS REGISTER U106

RAM MICRO-INSTRUCTION REGISTER U76 · U86

RAM CIRCUITS DATA

BIT 19 · BIT 18 · BIT 22 · BIT 23 · BIT 8 · BIT 9 · BIT 21 · BIT 16 · BIT 17 · BIT 20 · BIT 12 · BIT 10

IOB4 · IOB7 · IOB6 · IOB1 · IOB0 · IOB2 · IOB3 · IOB5 · IOB11 · IOB13 · IOB14 · IOB15 · IOB10 · IOB9 · IOB8 · IOB12

NOTES:

1. RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN UF UNLESS OTHERWISE SPECIFIED.

SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R8, R11, and R18

A 1K · B 1K · C 1K · D 1K · E 1K · F 1K · G 1K

SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R1, R9, R10, and R12

A 500 · B 500 · C 500 · D 500 · E 500 · F 500 · G 500

DWG REV A (SHEET 1 OF 3)

SRQ 19 · IOB 57 54 56 58 12 8 9 10 · IOB 74 65 61 60 15 14 13 11 · IOB 51 45 41 35 5 3 2 0 · 38 53 52 42 1 6 7 4 · PRH 23

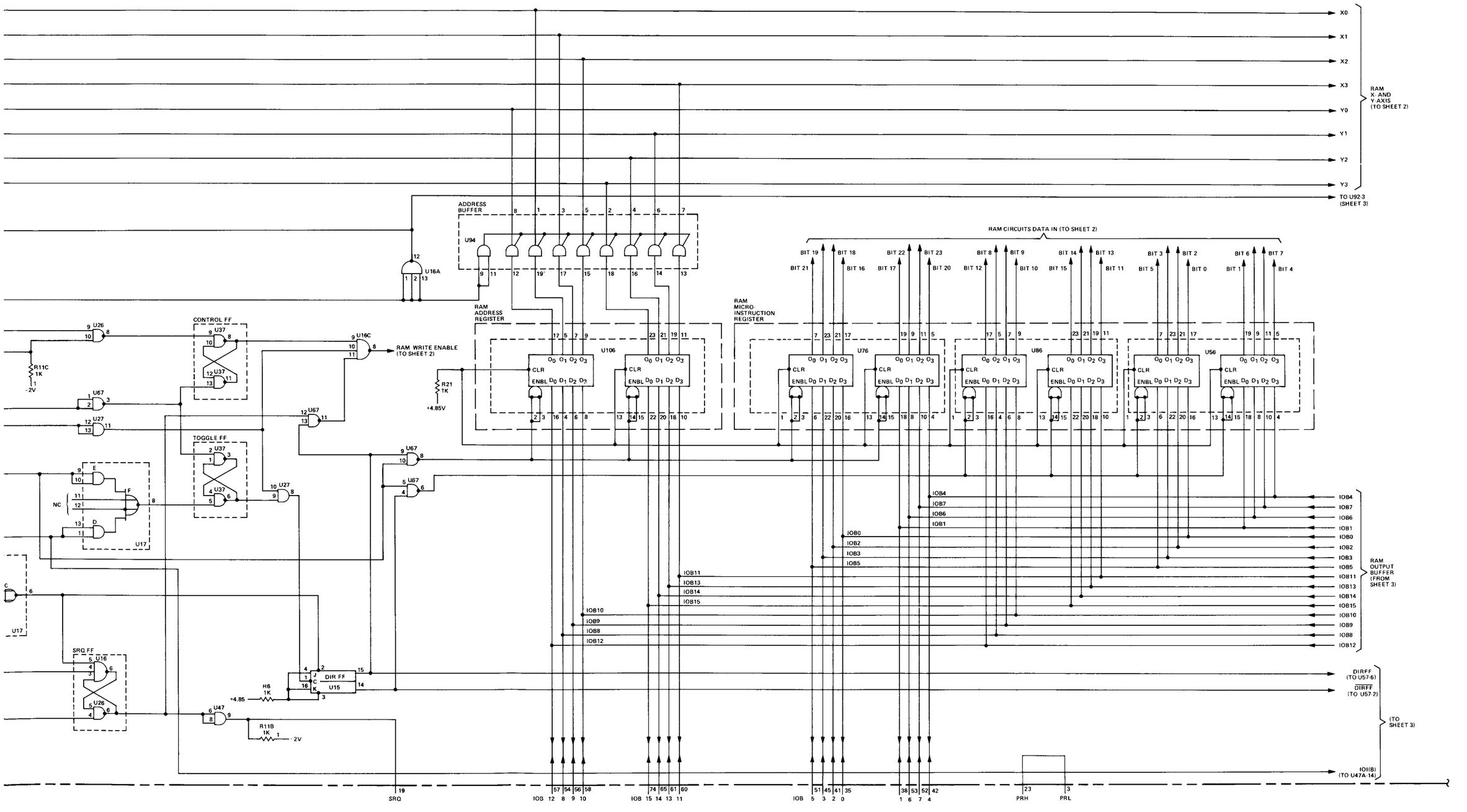

Figure 4-2. Writeable Control Store PCA, Parts Location and Schematic Diagrams (Sheet 1 of 3)

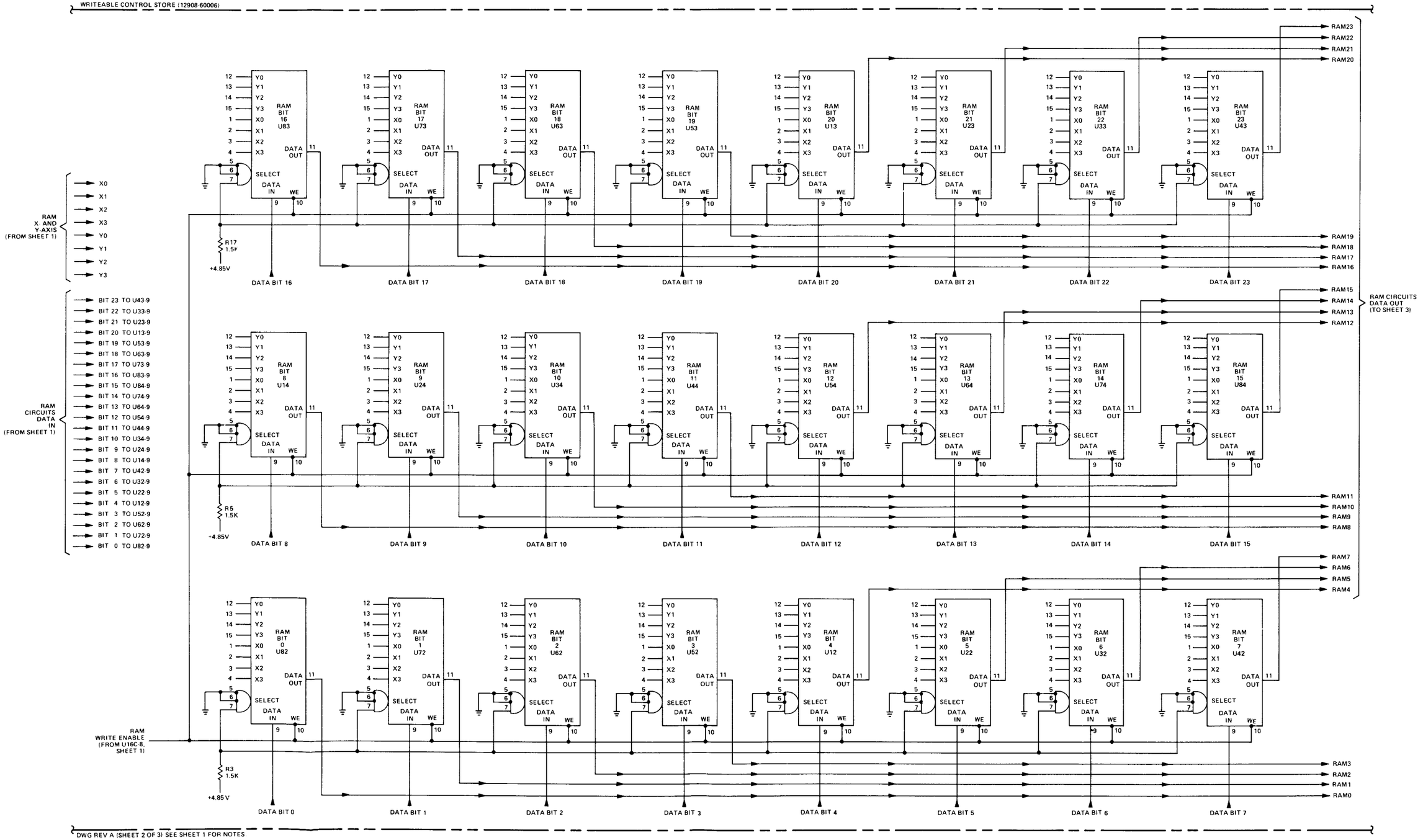

Figure 4-2. Writeable Control Store PCA, Parts Location and Schematic Diagrams (Sheet 2 of 3)

WRITEABLE CONTROL STORE (12908-60006)

RAR9 J1-48 RAR8 J1-46 RAR11 J1-20 RAR10 J1-18

RAM CIRCUITS DATA OUT (FROM SHEET 2)

RAM23 RAM22 RAM21 RAM20 RAM19 RAM18 RAM17 RAM16 RAM15 RAM14 RAM13 RAM12 RAM11 RAM10 RAM9 RAM8 RAM7 RAM6 RAM5 RAM4 RAM3 RAM2 RAM1 RAM0

(FROM SHEET 1)

DIRFF (U15-15)

DIR FF (U15-14)

IOI(B) (FROM U27-3)

+4.85V

R7 464

U57 R1 1K

U57 R2 1K

R15 215

R13 215

-2V

U21

U41

U46 U45 U35 U36 U97 U77 U87 U107

RAM OUTPUT BUFFER

(TO SHEET 1)

IOB4 IOB7 IOB6 IOB1 IOB0 IOB2 IOB3 IOB5 IOB12 IOB8 IOB9 IOB10 IOB15 IOB14 IOB13 IOB11

+4.85

R10A 464 R10B 464 R10C

DWG REV A (SHEET 3 OF 3) SEE SHEET 1 FOR NOTES.

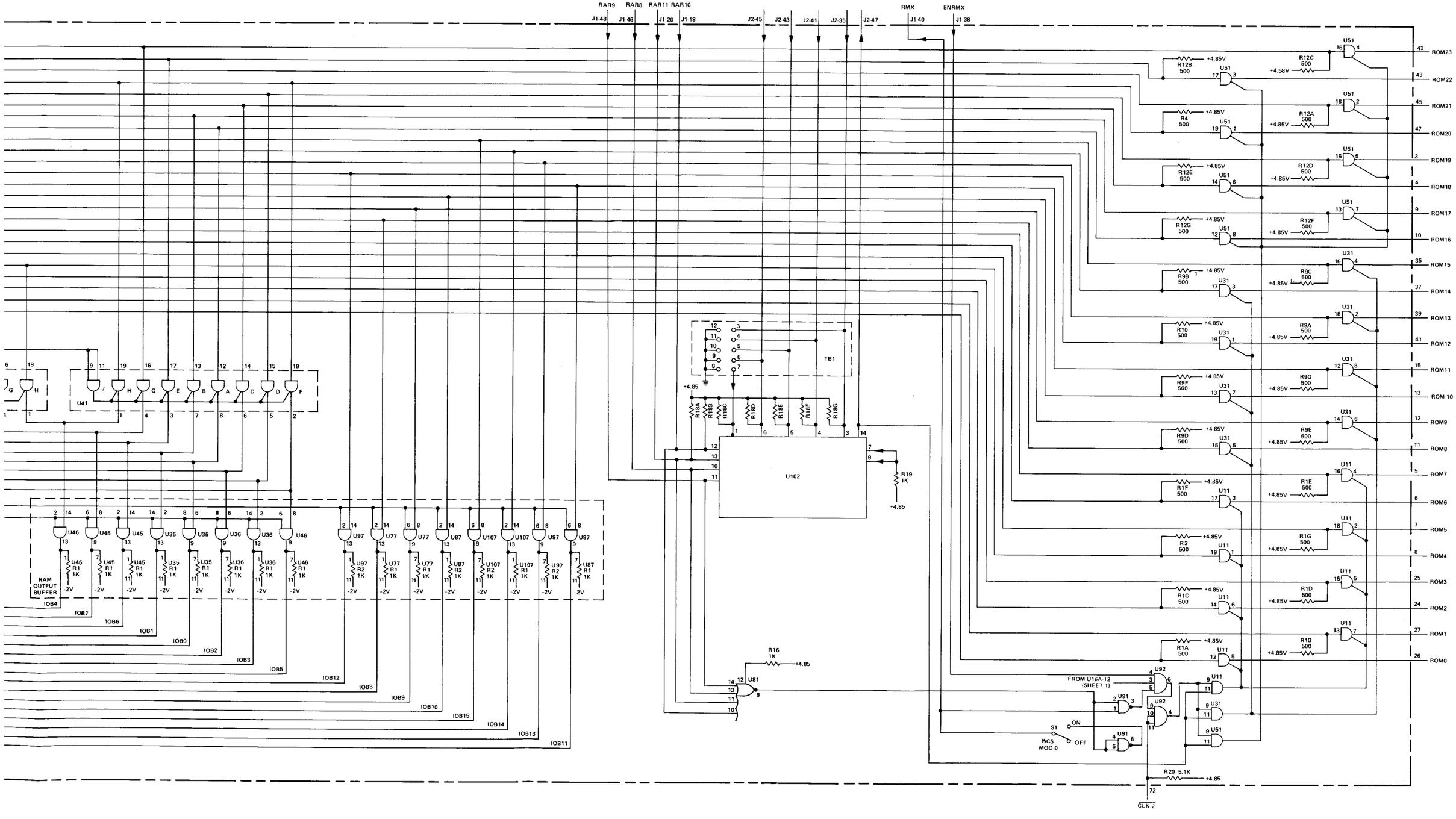

Figure 4-2. Writeable Control Store PCA, Parts Location and Schematic Diagrams (Sheet 3 of 3)

REPLACEABLE PARTS

SECTION V

5-1. INTRODUCTION.

5-2. This section provides information for ordering replacement parts for the HP 12908B Writeable Control Store Interface Kit. Table 5-1 lists the kit parts. Table 5-2 lists parts in numerical order by HP part numbers and gives the total quantity for each replaceable part in the interface kit. Table 5-3 lists the code numbers of the various manufacturers of the replaceable parts. A replaceable parts list (table 4-1) and parts location diagram (figure 4-2) for the PCA are provided in section IV of this manual.

5-3. Tables 4-1 and 5-2 provide the following information for each replaceable part:

a. Reference designation of the part (table 4-1 only). (Refer to table 5-4 for an explanation of the reference designations used in the REFERENCE DESIGNATION column.)

b. Hewlett-Packard part number.

c. Description of the part. (Refer to table 5-4 for an explanation of the abbreviations used in the DESCRIPTION column.)

d. A five-digit code identifying the manufacturer of the part. (Refer to table 5-3 for a code list of manufacturers.)

e. Manufacturer's part number.

f. Total quantity (TQ) of each part used in the kit or assembly (table 5-2 only).

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Refer to the list at the back of this manual for addresses. Specify the following information for each part ordered:

a. Identification of the kit or assembly containing the part.

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation for each part (if applicable).

Table 5-1. Writeable Control Store Interface Kit Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
12908-60006*	Writeable Control Store Interface PCA	28480	12908-60006	1
12908-60008	Writeable Control Store Jumper Board Assembly	28480	12908-60008	1
12908-90011	Operating and Service Manual	28480	12908-90011	1

*Option 001 consists of one PCA and jumper board assembly, part no. 12908-60003.

Table 5-2. Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0150-0121	CAPACITOR, cer, 0.1 µf, -20% + 80%, 50 Vdcw	13606	5C50B1-CML	6
0160-2055	CAPACITOR, cer, 0.01 µf, -20% + 80%, 100 Vdcw	13606	C023F101F103ZS	14
0180-0197	CAPACITOR, fxd, elect, 2.2 µf, ±10%, 20 Vdcw	56289	150D225X9020A2-DYS	4
0360-0294	TERMINAL	88245	2010B-2	7
0698-0082	RESISTOR, fxd, flm 464 ohms, 1%, 1/8W	28480	0698-0082	1
0698-3441	RESISTOR, fxd, flm, 215 ohms, 1%, 1/8W	19701	MF4CT-0	2
0698-5852	RESISTOR, fxd, flm, 500 ohms, 1%, 1/8W	28480	0698-5852	3
0757-0280	RESISTOR, fxd, flm, 1K, 1%, 1/8W	19701	MF4CT-0	4
0757-0427	RESISTOR, fxd, flm, 1.5K, 1%, 1/8W	19701	MF4CT-0	3
0757-0438	RESISTOR, fxd, flm, 5110 ohms, 1%, 1/8W	28480	0757-0438	1
1810-0030	RESISTOR NETWORK, 1K, 5%, 0.15W	13606	200C1618-CRR	3
1810-0037	RESISTOR ARRAY, cermet, 1K, 2%, 1-3/4W per array	28480	1810-0037	1
1810-0055	RESISTOR NETWORK, 10K, 5%, 0.125W	28480	1810-0055	1
1810-0080	RESISTOR NETWORK, 500 ohms, 5%, 0.15W	13606	200 Series	4
1820-0141	INTEGRATED CIRCUIT, TTL, quad 2-input AND gate	04713	SC7514PK	1
1820-0370	INTEGRATED CIRCUIT, TTL, quad 2-input NAND gate	01295	SN4478	4
1820-0371	INTEGRATED CIRCUIT, TTL, triple 3-input NAND gate	01295	SN4479	1
1820-0372	INTEGRATED CIRCUIT, TTL, triple 3-input AND gate	01295	SN4480	2
1820-0377	INTEGRATED CIRCUIT, TTL, dual 2-wide, 2 input AND/OR invert gate (expandable)	01295	SN4485	1
1820-0538	INTEGRATED CIRCUIT, TTL, dual 4-input NAND gate	28480	1820-0538	1
1820-0706	INTEGRATED CIRCUIT, TTL, 5-bit comparator	28480	1820-0706	1
1820-0715	INTEGRATED CIRCUIT, TTL, high speed dual edge-triggered J-K FF	01295	SN33510	1
1820-0742	INTEGRATED CIRCUIT, TTL, dual 4-bit latch FF	17803	SL17869	4
1820-0755	INTEGRATED CIRCUIT, TTL, 8-bit driver non-inverting	28480	1820-0755	3
1820-0759	INTEGRATED CIRCUIT, TTL, 8-bit receiver, non-inverting	28480	1820-0759	4
1820-0956	INTEGRATED CIRCUIT, TTL, dual 2-input AND buffer	17803	SL3459	10
1820-0988	INTEGRATED CIRCUIT, TTL, 256-bit read/write memory	17803	SL40850	24
1200-0474	SOCKET, integrated circuit, 14 pin	28480	1200-0474	1
3101-1213	SWITCH, DPST-DB, 0.5a, 28 Vdc	81640	T8001	1
5060-8342**	JUMPER ASSEMBLY, WCS PCA	28480	5060-8342	1
12908-60003*	Writeable Control Store Jumper Board Assembly (Option 001 only)	28480	12908-60003	1
12908-60006*	Writeable Control Store Interface PCA	28480	12908-60006	1
12908-60008	Writeable Control Store Jumper Board Assembly	28480	12908-60008	1
12908-90011	Operating and Service Manual	28480	12908-90011	1

*Option 001 consists of 12908-60006 PCA and 12908-60003 Jumper Board Assembly.

**This assembly is TB1 with all jumpers installed.

Table 5-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas	19701	Electra Mfg. Co.	Independence, Kan.
04713	Motorola Inc., Semiconductor Prod. Div	Phoenix, Ariz.	28480	Hewlett-Packard Co.	Palo Alto, Cal.
13606	Sprague Electric Co., Transistor Div.	Concord, N.H.	56289	Sprague Electric Co.	N. Adams, Mass.
17803	Fairchild Camera and Instrument Corp., Semiconductor Div.	Mountain View, Cal.	81640	Control Switch Div. Control Co. of America	Folcroft, Pa.
			88245	USECO Div. Litton Industries	Van Nuys, Cal.

MANUAL PART NO. 12908-90011
MICROFICHE PART NO. 12908-90012

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